EDUCATIONAL EXPERIMENTS WITH NON-LINEAR FPAA CONFIGURABLE ANALOG MODULES

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The paper discusses the structure and mode of operation of the non-linear Configurable Analog Modules of AN221E04 Chip of Anadigm Inc. Their transfer characteristics are given, as well as the requirements for the clock frequencies and the limitations for the input and output signal levels. Through different illustrative and convincing experiments, realized by the specialized AnadigmDesigner2 software simulator, are demonstrated the resources of the examined blocks for multiplication, division and square root extraction. The investigated circuits are practically implemented on a specialized platform of the company and their efficiency is verified. An estimation of the precision is made.

Keywords: Field Programmable Analog Array (FPAA), Configurable Analog Module (CAM), Analog Multiplier/Divider, Switched-Capacitor Circuit

I. INTRODUCTION

In analog circuitry it is often necessary non-linear operations with analog quantities (e.g. multiplication, division, square root extraction etc.) to be implemented.

The analog arrays of Anadigm are very appropriate for the realization of non-linear mathematical operations. Field Programmable Analog Arrays (FPAAs) are an analog equivalent to the Field Programmable Gate Arrays (FPGAs). They bring together the three most powerful design trends from the digital world – design automation, field-programmable ICs, and real-time updating – into a new platform for analog design. With Anadigmvortex (the latest-generation Field Programmable Analog Array product family) designers can construct complex analog functions with the drag-and-drop AnadigmDesigner®2 EDA tool and adjust functionality in automatically generated C-code [1]. With dynamically reconfigurable Field Programmable Analog Arrays, now analog functions can be controlled, updated, and manipulated by the system processor in real time – a breakthrough that brings analog into the system mainstream. Moreover, reconfigurable Field Programmable Analog Arrays structures include different Configurable Analog Modules (CAMs) – multiplier, divider, square root and transfer function. The presence of such blocks with their ability for fast and simple reconfiguration makes them especially suitable for the above-mentioned aim.

The paper proposes educational experiments with configurable non-linear modules of AN221E04 Chip of Anadigm Inc. To this aim the operation of the multiplier, divider and square root extraction modules are investigated. The obtained results are applied in the design and implementation of two-parameter test circuit.

II. EXPERIMENTS FOR INVESTIGATION OF NON-LINEAR CAMS OF FPAA

II.1 Examination of Multiplier CAM

The basic circuit element for the multiplier CAM is a half-cycle offset compensated gain stage, shown in Fig. 1.

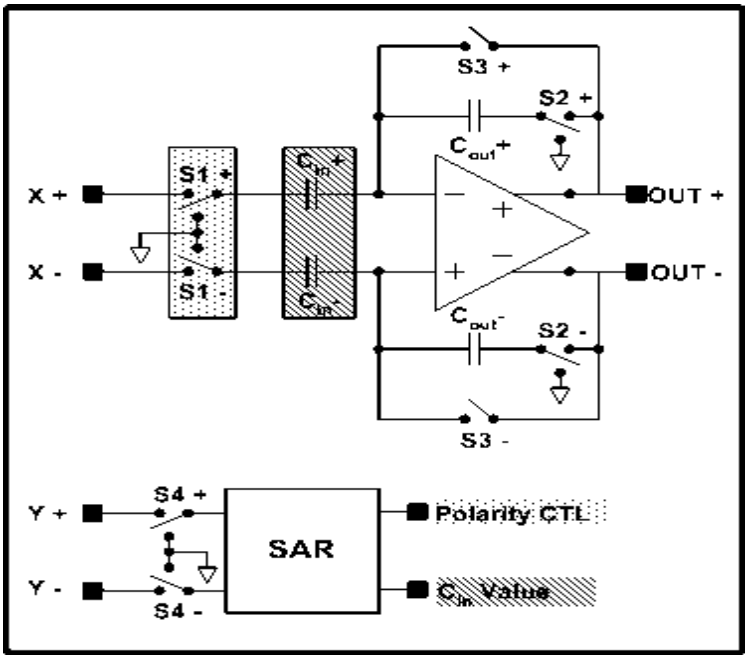


Fig. 1. Internal structure of Multiplier CAM.

This basic gain stage has the linear transfer function:

$$U_{OUT} = \frac{C_{IN}}{C_{OUT}} * U_{INX}, \quad (1)$$

where C_{IN} is the input capacitance and C_{OUT} is the feedback capacitor. The actual values of C_{IN} and C_{OUT} (ranging from 0 to 255 units) are determined by the data held in RAM local to the gain stage.

Within this circuit:

- switches S1 and capacitors C_{IN} sample the input voltage;
- switches S2 and capacitors C_{OUT} provide a feedback path;
- switches S3 are used to reset the circuit, thus operating antiphase to switches S2.

While the S3 switches are closed, the output of the gain stage is nominally zero.

The second input to the CAM is U_{INY} (shown as Y+ and Y- in Fig.1). This input is sampled by the ADC (SAR) within the CAM. The result at the ADC output is an eight bit digital word (D_{OUT}) corresponding to the U_{INY} value. The format of D_{OUT} is sign+magnitude, i.e. the polarity of D_{OUT} sets the first bit of D_{OUT} and the subsequent seven bits represent the magnitude of U_{INY} relative to the on-chip reference voltages. The full-scale input range of the SAR is ±3V, based on the internal reference voltage [2]. Input voltages that exceed this full-scale range will produce results as if the input voltage was equal to the full-scale. If $U_{INY} = +V_{REF}$, then D_{OUT} = 01111111 and if $U_{INY} = -V_{REF}$, then D_{OUT} = 11111111.

Through the value of C_{OUT} is determined a multiplication factor M, which results in the following relation for the transfer function [2]:

$$U_{OUT} = M * U_{INX} * U_{INY}(\text{quantized}) \quad (2)$$

For four quadrant operation the sign bit of D_{OUT} is then used to invert (or not) the phasing of the input switches (S1). Thus, the amplifier works as inverting or non-inverting and the sign of U_{INY} is considered.

The two inputs have the same effect on the output voltage to a first order, but in fact, there are a number of significant differences in practice. For instance, the X input is fed directly into the gain stage, but the Y input is fed into the ADC. The Y input is thus 'quantized' to 25mV (i.e. 6V/256) [3]. The resolution of the X input is better than that of the Y input, and the user should bear this in mind to extract the maximum performance from the CAM. Consequently, it is recommended that the higher input voltage (U_{INX} or U_{INY}) is connected to the Y input.

The multiplier CAM is constructed so that the Y input is sampled on phase 1 of the given clock. As already mentioned, for four quadrant multiplier, the input switches S1 of Fig. 1 will sample the value of U_{INX} on either phase 1 or phase 2, which is determined by the polarity of U_{INY}.

A sample and hold module may be added to the X inputs (sample and hold on). This is necessary since the phase of the X input branch cannot be determined in advance and the $\Delta\varphi$ symbol on the multiplier CAM symbol denotes this fact. This ensures that the X input to the CAM is valid on both phases of the clock or the input signal may be missed on one of the two possible phases. However, when the value of U_{INX} is constant or it changes only slowly relative to the clock frequency, the addition of that module is not needed (sample and hold off). The latter is also valid when it is clear on which phase will be sampled the value of U_{INX}.

The ADC in the multiplier CAM is based on a successive approximation algorithm. It takes nine steps to convert U_{INY} to the appropriate data output D_{OUT}, and a further cycle to write the data to the appropriate RAM location(s). A number of extra clock cycles are usually necessary to allow setting of the analog components before the multiplier takes its next sample of U_{INX}. Consequently, two clocks are required for the multiplier CAM, a relatively slow one for the gain stage and a second faster one (16 times faster) for the SAR ADC.

The 16:1 clock ratio required by the CAM arises from the need to allow time for the SAR ADC to convert U_{INY} to D_{OUT} with some settling time at the end.

To allow an accurate conversion of the Y input, the voltage on this input should not change during the several steps of the conversion. If it does change, an erroneous output may be produced.

To ensure this does not happen, the user must see that either one of two conditions are satisfied [3]:

1. The voltage on U_{INY} changes only slowly relative to the clock rate. It is recommended that no more than 10mV of gradual change should be allowed during a

slow clock period. This amounts to ½ LSB of the ADC and will usually not give significant errors.

2. A sample and hold circuit is connected to the U_{INY} terminal to hold the voltage steady during conversion. This sample and hold should be clocked with the slow clock of the multiplier CAM to ensure proper synchronization.

The second option has the advantage of producing better buffering of the Y input and allows the multiplier to be clocked at a higher rate than the suggested defaults.

The multiplier gain stage is a circuit, which has a valid output for only half the time, i.e. it is a half-cycle circuit. An addition of a sample and hold CAM to the multiplier output will produce a full-cycle output if required.

Fig.2 demonstrates the results from the operation of the Multiplier CAM. The waveforms of the input and output signals are shown. The X and Y inputs are connected with rectangular impulses with amplitudes of 2 V and 1 V, respectively, which allows the operation of the multiplier as four quadrants one to be demonstrated. The third and fourth waveforms illustrate the input voltage with and without output sample and hold. The value of U_{OUT} completely follows the relation (2), while taking into account that M=1.49.

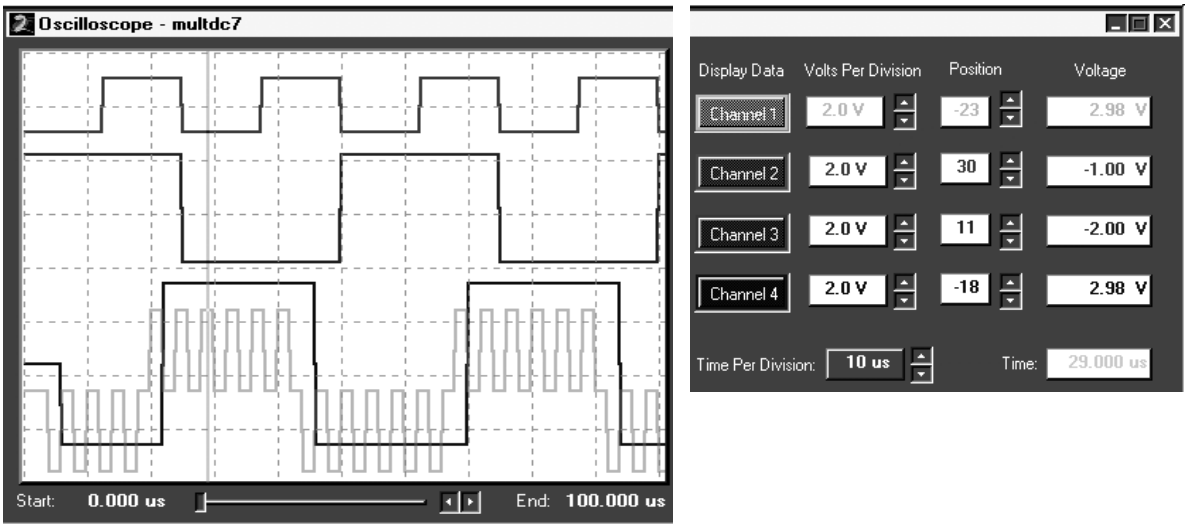


Fig.2 Results from the operation of the Multiplier CAM.

II.2 Examination of Divider CAM

The internal structure of this module is similar to the Multiplier CAM. The transfer function is [2]:

$$U_{OUT} = \frac{U_{INX}}{U_{INY}(\text{quantized}) * D}, \tag{3}$$

where D is the Divisor Factor. Fig.3 demonstrates the basic structure for the implementation of a Divider CAM. U_{INY} is a DC input so the transfer function of U_{INX} can be clearly seen on Fig.4. The output of this CAM is half cycle .The full-scale output range of the Divider is ± 4 V [2]. Addition of a sample and hold to the output will produce a full-cycle output if required.

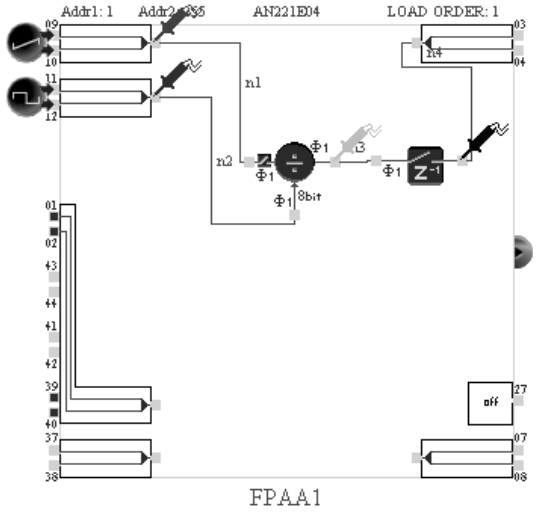


Fig.3.Basic structure for implementation of Divider CAM.

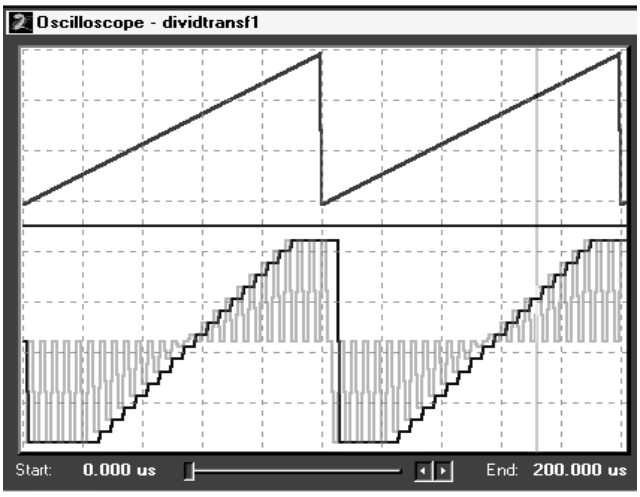


Fig.4 Results from the operation of the Divider CAM.

II.3 Examination of Square Root CAM

The transfer function for this CAM is [2]:

$$U_{OUT} = \text{sign}(U_{IN}) * \sqrt{U_{IN}} \tag{4}$$

The transition to a new output level will not be instantaneous since the feedback path produces a low pass filter. Due to the nonlinear feedback gain, the corner frequency of this filter is not constant but is approximately proportional to the output voltage. Fig.5 shows the experimental transfer characteristic of this module.

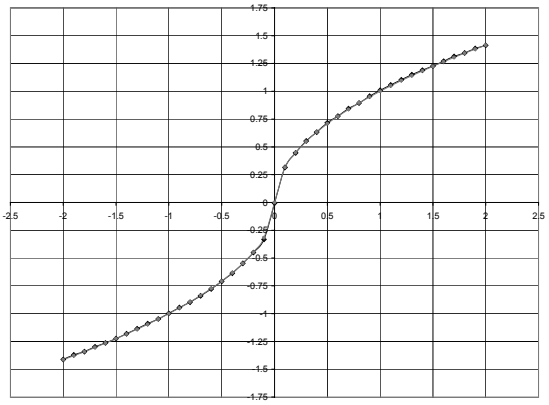
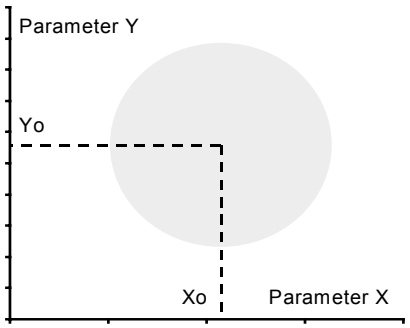


Fig.5 Experimental transfer characteristic of Square Rroot CAM

III. EXAMPLE: TWO-PARAMETER TEST CIRCUIT

Below is proposed a simple and elegant 2-parameter test circuit that uses FPAA. By the realization of the mathematical operations shown on Fig.6, this circuit checks whether the values of the Parameter X and Parameter Y come into the denoted circle area.



"TRUE":
If $(X-Xo)^2+(Y-Yo)^2<R^2$

"FALSE":
If $(X-Xo)^2+(Y-Yo)^2>R^2$

Fig. 6. The circle area of 2-parameter test circuit

Fig.7 shows the FPAA application of this circuit and Fig.8 presents the results from the investigation.

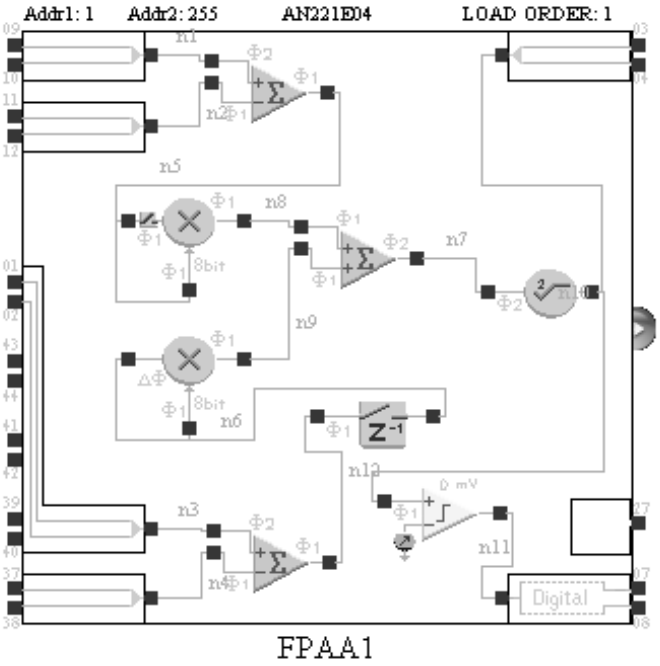


Fig.7. FPAA implementation of the test circuit.

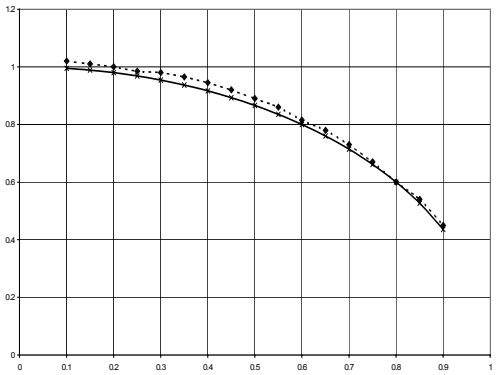


Fig.8.Results from practical examination of the circuit.

IV. CONCLUSION

The paper discusses different training experiments with multiplier, divider and square root extraction CAMs of Anadigm. The investigated circuits are practically implemented on a specialized platform [1] of the company and their efficiency is verified. The obtained results are applied in the design and implementation of two-parameter test circuit, which uses two multipliers and square root extraction CAMs.

The presented results will be applied in research and education.

V. REFERENCES

[1] Anadigm Inc. Field Programmable Analog Arrays – User Manual. 2002.
[2] Anadigm Inc. Documentation. www.anadigm.com.
[3] Anadigm Inc. Desing Brief 208. 2002.