USING VHDL – AMS IN VLSI DESIGN LABORATORY EXERCISES

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VHDL support only nine values of discrete signals. The most of today's electronic systems can received information in which at least one is analog signal. In order to process continues signal it has to be converted to digital one. It is doing with ADC (Analog to digital converter). The concrete design can require some of digital signals to be converted to analog types. It is doing with DAC (Digital to analog converter). In order to use this types of signals or to model ADC or DAC electronic elements, we have to apply different languages. VHDL – AMS (Analog and mixed signal) has been introduced to decrease number of used languages in the digital design. There is an extension of VHDL which is IEEE Standard 1076.1 – 1999. IEEE Standard 1076.1 – 1999 together with IEEE Standard 1076 – 1993 is informally known as VHDL – AMS.

Keywords: VHDL, VHDL - AMS, ADC, DAC

1. INTRODUCTION

In the VLSI (Very large scale integration) design laboratory exercises VHDL (Very high speed integrated circuit Hardware Description Language) [8] has been introduced in order to simulate, synthesize and implement concrete design examples. VHDL is an IEEE (Institute of electrical and electronics engineers) Standard 1076 – 1993. In exercises has been installed and used ModelSim – Altera and Quartus® II software programs as well as UP (University program) 2 development kit [3]. We have applied in the lab exercises above mentioned software and hardware tools because of entering in Altera Corporation University program.

VHDL (especially std_logic_1164 package which resides in the IEEE library) support only nine values of discrete signals – logic one or logic zero, third (Z) state, unknown (X) state, etc. The most of today's electronic systems can received information in which at least one is analog (continues) signal. As example the signal is possible to be from analog sensor [2]. In order to process continues signal it has to be converted to digital one. It is doing with ADC (Analog to digital converter). The concrete design can require some of digital signals to be converted to analog types. It is doing with DAC (Digital to analog converter). In order to use this types of signals or to model ADC or DAC electronic elements, we have to apply different languages.

With VHDL language it is possible to model ADC but it is time consuming process. As an example of previous sentence VHDL model of TSL 230 [7] sensor has been introduced.

2. TSL 230 VHDL MODEL

TSL 230, TSL 230A, and TSL 230B programmable light-to-frequency converters combine a configurable silicon photodiode and a current-to-frequency converter on single monolithic CMOS integrated circuits. The output can be either a pulse train or a square wave (50% duty cycle) with frequency directly proportional to light intensity. Device sensitivity is selectable in three ranges, providing two decades of adjustment. The full-scale output frequency can be scaled by one of four preset values. All inputs and the output are TTL compatible, allowing direct two - way communication with a microcontroller for programming and output interface. An output enable (oe) is provided that places the output in the high-impedance state for multiple-unit sharing of a microcontroller input line. In order to model correctly TSL230 has been used information from tables, which are part of the technical documentation provided by TAOS Inc. In addition, has been also used as source of technical information diagrams provided by TAOS Inc. in TSL 230 data sheet [7].

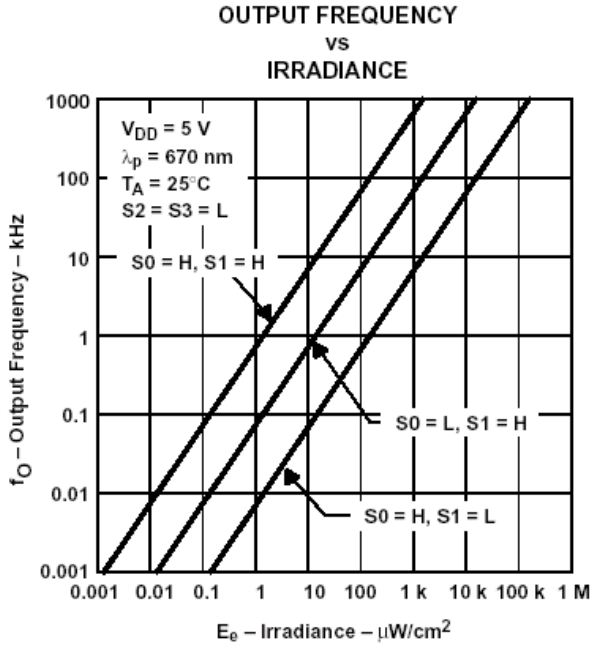

Fig. 1

On the Fig. 1, it is shown the most important diagram for TSL 230 – fo = f (E_e).

E_e is analog value but fo (output frequency) is digital value – we have to count the number of produced pulses for a given time in order to receive binary code corresponding to E_e value. To be more precise we have to add VHDL model of a counter, and a VHDL control circuit, which will be responsible for starting, resetting and finishing analog to digital conversion.

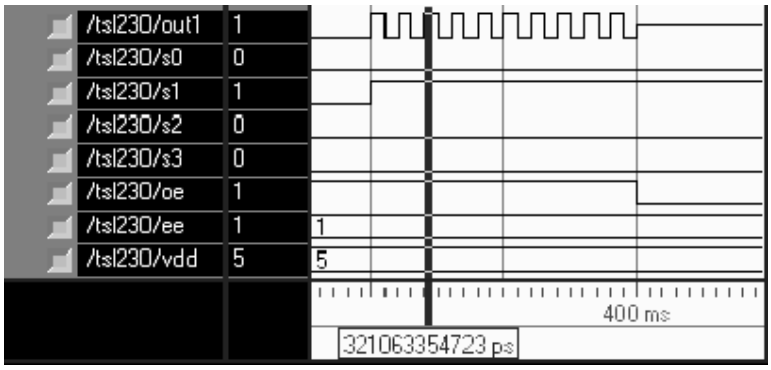

Fig. 2

In order to build TSL 230 VHDL model we have started model function of oe signal. If this signals is L (Logic zero) output named out is going to high-impedance state (Z state). If oe is equal to H (Logic one) then TSL 230 is working properly. This situation we are able to see on the next ModelSim-Altera 5.7e diagram. The used VHDL simulator is received as a donation because of entering in Altera University Program (UP) [3]. In the above waveforms signal out1 is equal to signal out of the real device. The out is a keyword in VHDL and for this reason has not been used as a name of the TSL 230 output pin in the VHDL model.

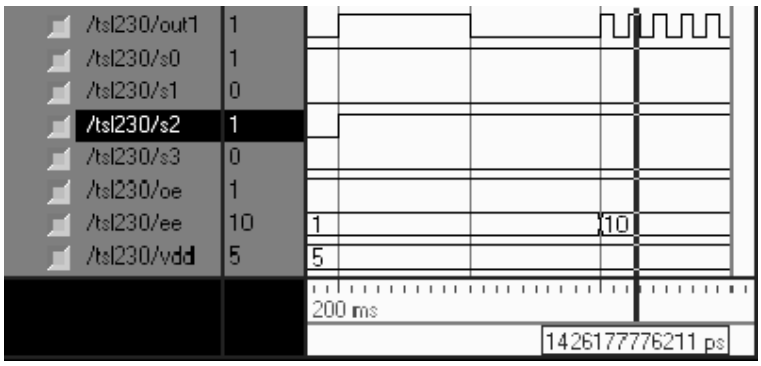

Fig. 3

After that we have modeled functions of the signals s0, s1, s2 and s3. Depends on concrete combination we are able to see output pulses with different frequencies.

We are able to see from Fig. 4 that when s0 and s1 are equal to L, there are no output square pulses. Then we have started changing the value of irradiance (Ee) to check output frequency values. Has been verified linearity of the dependency between Ee, s0, s1, s2 and s3 and output frequency. More information about Ee and another different light quantities we are able to find in [1, 6].

On the Fig. 3, Fig. 4 and Fig. 5 are shown the received results by simulation after changing value of Ee, s0, s1, s2 and s3.

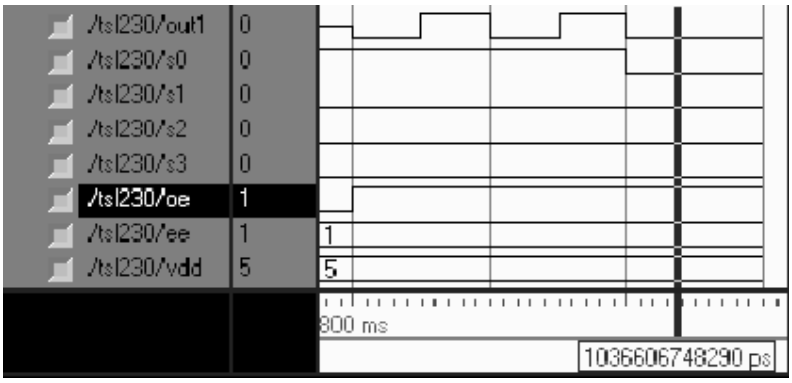

Fig. 4

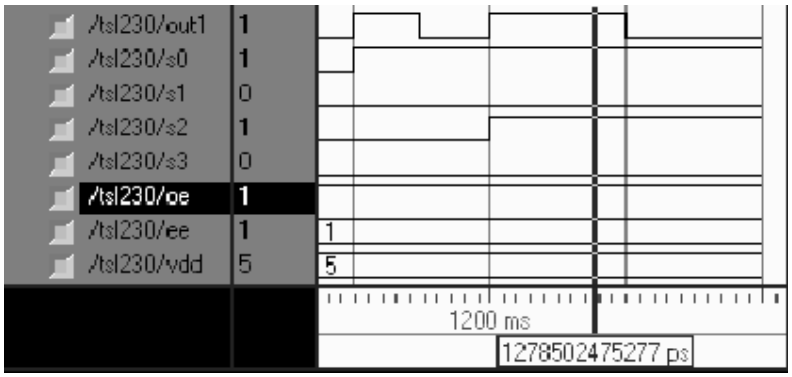

Fig. 5

3. VHDL – AMS AND SIMPLORER® 7.0 STUDENT VERSION – BASICS, WORKING ALGORITHM, VHDL – AMS MODEL AND SIMULATION RESULTS

VHDL – AMS (Analog and mixed signal) [8]has been introduced to decrease number of used languages in the digital design. There is an extension of VHDL which is IEEE Standard 1076.1 – 1999. IEEE Standard 1076.1 – 1999 together with IEEE Standard 1076 – 1993 is informally known as VHDL – AMS. VHDL – AMS is a strict superset of IEEE Standard 1076 – 1993 because any model valid in VHDL 1076 is a valid in VHDL – AMS and yields in the same simulation results. An example of the tested 4 – bit ADC is shown on the Fig. 6 [4].

Simplorer [4] is a software package used to design and analyze complex technical systems. Simulation models can contain electrical circuit components of different physical domains, block model elements, and state machine designs. Simplorer's simple graphical interface allows easy setup of even complex designs. Simplorer's fast and stable simulation algorithms reduce design time and provide reliable results.

In order to work with Simplorer ® 7.0 Student version, we have to complete 7 tasks – to place components, to connect components, to define properties, to set

output definitions, to display quantities on sheet, to set simulation parameters and the final step is to start simulation.

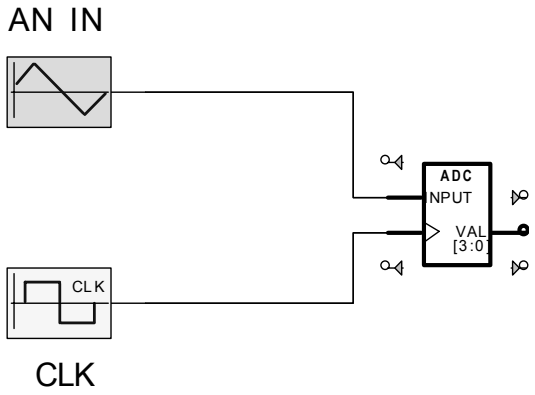

Fig. 6

On the next line is introduced 4 – bit ADC modeled with VHDL – AMS language.

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.ELECTRICAL_SYSTEMS.ALL;
ENTITY ADC IS
GENERIC (MIN : REAL := -1.0;
MAX : REAL := 1.0);
PORT (SIGNAL CLK : IN BIT := '0';
QUANTITY INPUT : REAL := 0.0;
SIGNAL VAL : OUT BIT_VECTOR(3 DOWNTO 0) := (OTHERS => '0'));
END ENTITY ADC;
ARCHITECTURE behav OF ADC IS
BEGIN
PROCESS
VARIABLE delta_v : REAL := 0.0;
VARIABLE input_hold : REAL := 0.0;
BEGIN
WAIT ON CLK;
delta_v := MAX - MIN;
input_hold := INPUT - MIN;
IF (CLK'EVENT AND CLK = '1') THEN
FOR i IN 3 DOWNTO 0 LOOP
delta_v := delta_v / 2.0;
IF input_hold >= delta_v THEN
VAL(i) <= '1';
input_hold := input_hold - delta_v;
ELSE
VAL(i) <= '0';
END IF;
```

```
END LOOP;
END IF;
END PROCESS;
END ARCHITECTURE;
```

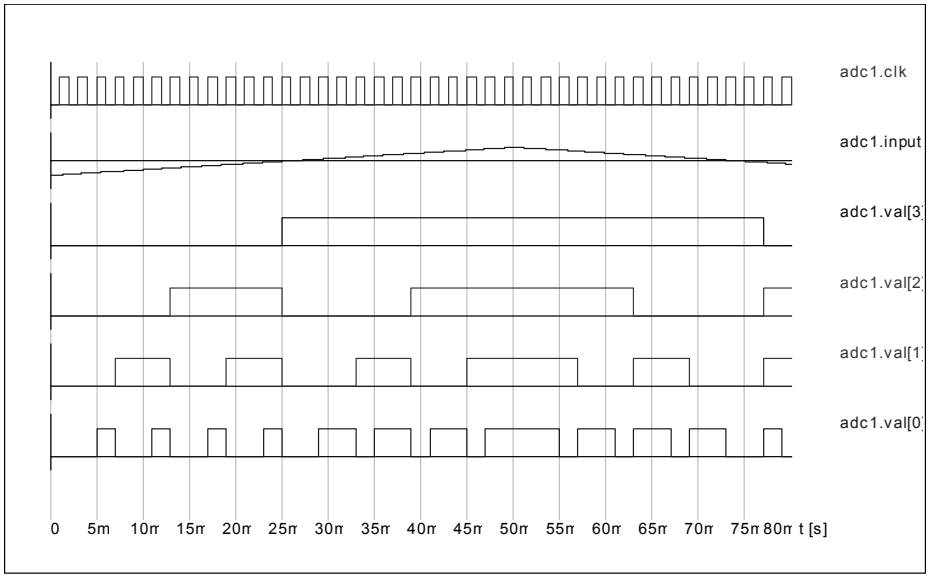

Fig. 7

On the Fig. 7 are introduced results received from simulation of 4-bit ADC modeled with VHDL – AMS by Simplorer ® 7.0 Student version.

4. CONCLUSIONS

- The proposed VHDL TSL 230 model has been verified using ModelSim-Altera 5.7e. The simulation results have shown that model is working properly;
- We have proposed to use VHDL – AMS in order to model ADCs and DACs;
- The simulation results of 4-bit ADC VHDL – AMS model has been received using Simplorer ® 7.0 Student version simulator;

5. REFERENCES

[1] Ryer A., *Light measurement handbook*, Technical Publications Dept.International Light Inc., USA, 1997.

[2] Tetelin. A, H.Levi, B.Mongellaz and C.Pellet, *Behavioral modeling of a humidity sensor using an analog hardware description language*, Proceedings of Modeling and Simulation of Microsystems conference, pp. 140- 143, Puerto Rico – USA, 2002

[3] http://www.altera.com

[4] http://www.ansoft.com

[5] http://www.eb.uah.edu/~wells

[6] http://www.instrumentsystems.de

[7] http://www.taosinc.com

[8] http://www.vhdl.org