SOME PECULIARITIES OF THE RESISTOR LAYOUT DESIGN IN CAD SYSTEMS

Valentin Hristov Videkov[1], Rossen Ivanov Radonov[2], Stefan Dimitrov Donchev[3]

Faculty of Electronic Technologies, Technical University of Sofia, 8 St. Kl. Ohridski blvd.,1000 Sofia, Bulgaria, phone[1]: +359 2 965 3101, phone[2]: +359 2 965 3115[2], Institute of Electronic BAS Sofia, 7km bul. Tsarigradsko shose [3] e-mail[1]: videkov@tu-sofia.bg, e-mail[2]: radonov@ecad.tu-sofia.bg

This paper presents the results from the investigation of complex resistor layout design in CADENCE environment. Comparisons between the nominal values of resistors with equal length and different layout are shown. The values can differ depending on the complexity of the system. A method for visual demonstration of layout influence using popular software for analyses is proposed. The method is experimentally tested using thin-layer resistors with different layout. The results reveal a good coincidence and possibilities for the model's application.

Keywords: modelling, layout design, integrated circuits

1. INTRODUCTION

Contemporary integrated circuits are 100% designed using CAD systems like CADENCE [1,2]. Due to their functional complexity the monolithic ICs require usage of embedded capacitors and resistors. In some areas it is not possible to exclude such elements [3]. One of ICs' characteristics is the creation of resistors beneath the surface, in the semiconductor layers or intermediate levels. It is a common practice to create resistor bodies in non-special layers, which are result of other technological processes [4]. This imposes different lengths and shapes to be used, including bending in order to obtain different resistor values. Unlike hybrid ICs, where resistor trimming is not a problem [5], monolithic ICs are not capable of that.

2. THE OBJECTIVE

The design of ICs, containing differential stages, or other circuits for parallel signal processing forces the creation of identical and/or precise resistors. In this aspect it is necessary to know the resistor layout influence upon its value. The task is to study different resistor layout shapes, designed with the existing CADENCE Design Kit and develop a method for representation of this influence, using well-known means.

3. RESISTOR DESIGN IN CADENCE

Different Design kits have different layers defined for resistor layouts.

The basic design rules include usage of layers, which have known sheet resistance. As for the resistors extraction, their shape is limited to a couple of varieties. After drawing the resistor body, it is being surrounded by a special layer,

which is maximally tight to it. This layer does not participate directly in the technological process. The layer is used to define the resistor's boundaries, within which the resistance is being calculated.

The extraction and calculation rules are defined in the technology library of the Design Kit, which is tied to an existing technology. In this aspect the resistor design is always connected with a certain IC manufacturer, which has to supply the technology data.

4. EXPERIMENTAL LAYOUTS

Fig. 1 shows the basic layout groups with increasing length values were used to study the layout influence.

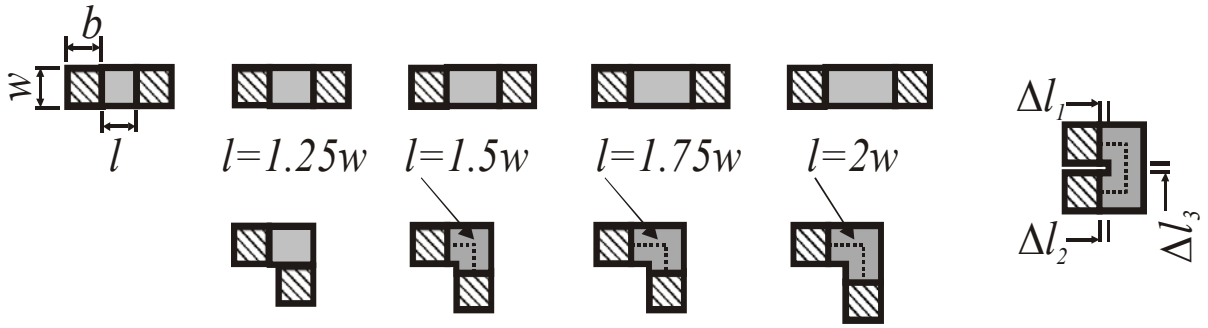

Fig. 1. Types of resistor layout shapes

These layouts form three basic shapes used for complex resistor layouts

5. CORRECTIONAL COEFFICIENTS

There are known correctional coefficients used in hybrid ICs technology, which can be applied to the abovementioned shapes [6]. The method is applied to resistance calculation of resistors with complex layout and arbitrary contacts' position. A comfort image and Jacob's elliptic function are used. There are two cases for the practice – a symmetrical Γ-like bending, where $l = 3w$ and a Π-like bending, where $l = 5w$, i.e. $\Delta l = w$.

The resistance in both cases is calculated as follows:

$$R_{\Gamma} = \kappa \frac{l}{w} R_s = \kappa n R_s = 2{,}56 \text{ R}_\text{s} \qquad \text{Equation (1)}$$

$$R_{\Pi} = \kappa \frac{l}{w} R_s = \kappa n R_s = 4.11 \text{ R}_\text{s} \qquad \text{Equation (2)}$$

This correction is needed because of the current lines torsion due to the current flows through the complex layouts.

There are shapes other than the mentioned in practice. One of the cases is when there is a bending with a gap less than the resistor's width w. It is needed to check to what extent CADENCE uses these corrections.

6. RESULTS OF RESISTORS' LAYOUT DESIGN.

in CADENCE is shown in fig. 2.

Fig. 2. Resistors in CADENCE environment.

Table 1 shows part of the values achieved with increasing lengths of the resistors.

Table 1.

No.	*l/w*	linear	Γ	Π
1	1	200	x	200
2	1,25	250	x	250
3	1,5	300	300	300

The results show that the educational version of the Design Kit does not hold an account of the current line torsion in complex shaped resistors. The students has to be aware of that and take it into consideration when designing their circuits. As it was states, the formulae, which are well-known from the literature, do not give corrections for all shapes. Methods for mathematical solving are being proposed, which are hard and not always demonstrative. A demonstrative method for all shapes is needed to be developed.

7. A MODEL OF THE LAYOUT SHAPE

There are modules for circuit analyses, which are embedded in the industry standard CAD systems. Therefore, if the layout shape could be represented by an electric circuit, which takes into consideration 3-D elements, we could analyse the process of current line torsion.

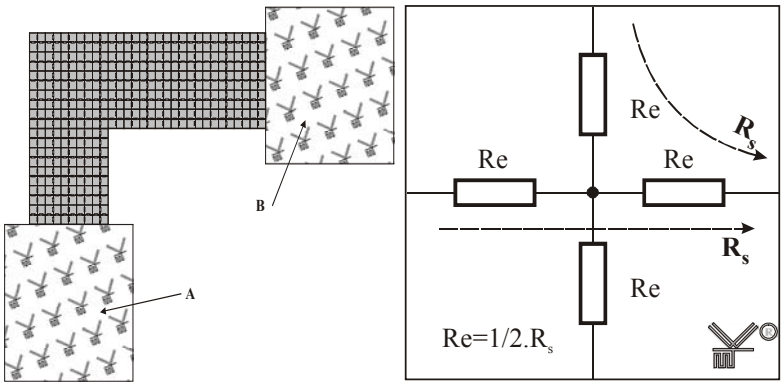

Fig. 3. Layout decomposition into elementary cells and a model of an elementary cell.

If we take into consideration only the 2-D elements, we can make the following representation of a resistor. The shape is decomposed into elementary cells. Each cell

can be replaced by a resistor which reflects the physical parameters of the layer. If we take that the sheet resistance is R_s ,then it must be constant when the current flows in the four directions of the cell. In that case the layout can be represented as interconnected cells (fig. 3). The electrical model of this layout is obtained by connecting the model of the elementary cell. One specific characteristic of its is that the end elements do not participate in the current flow and are not connected. The electrical circuit, which is obtained in that way, can be analysed with well-known software means. One of the contacts is accepted to have equal potential and connected to the ground. The other one is connected for example to 10 V power supply.

8. EXPERIMENTAL RESULTS

The first stage of the experiments was dedicated to the investigation of the current distribution in the resistor. This can be achieved by defining the current value in the separate resistors of the elementary cell. An indicator of the uneven current distribution is the current definition in different cross-sections. Fig. 4 shows the current distribution in the zone where the current flows into the contact. The cross-section is parallel to the contact and is made at the bending point.

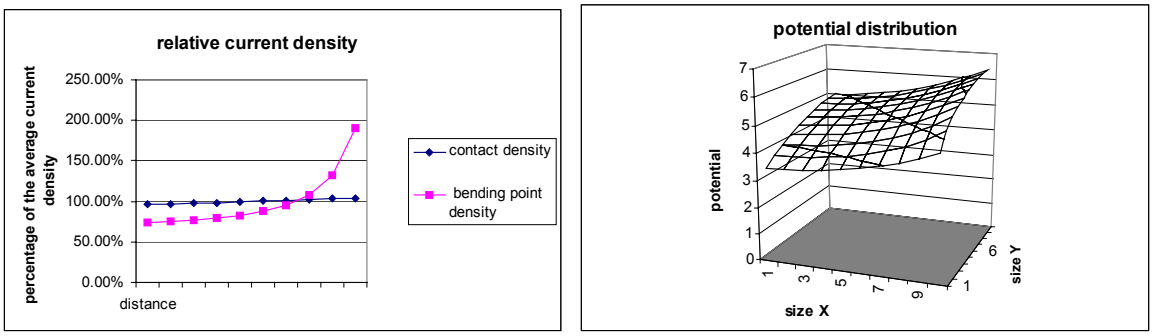

Fig. 4. Calculation of current distribution and potential at the bending point.

The second stage is related to the definition of the equivalent resistance of the model resistor and comparison to the experimentally measured one. The equivalent resistance is calculate by the formula:

$$R_E = \frac{10}{\sum_{1}^{n} I_e}, \qquad \text{Equation (3)}$$

where 10 is the supply voltage, I_e is the current through the relevant resistor of the elementary cell, and n is the number of elementary cells in the given cross-section. After that the difference between the two values is calculated.

9. VERIFICATION OF THE MODEL

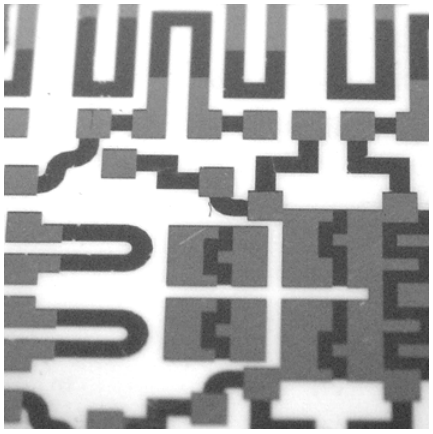

Fig. 5. Experimental resistors

An indicator for the model's precision is the comparison between the calculated and measured resistance values. Fig. 5 shows part of the thin-layer resistors prepared upon sital. The resistive layer is NiCr, which has a sheet resistance of 163 Ω/□. A Ni layer is deposed upon it, which serves as conductor. It can be easily soldered, which decreases its resistance. In this case we accept that the contact pads have equal potential, since their sheet resistance is over 1000 times smaller than that of the resistive layer. When the layout is decomposed into more than 6 elementary cells per square, the error between the calculated and measured values is less than 4%. The error derived from resistors' preparation is not taken into account. Similar results are obtained when measuring the potential distribution via a probe.

10. CONCLUSIONS

As a result of the experiments it has been noticed that some CADENCE Design Kits does not contain functions for calculation of complex layout resistors' resistance. Such kinds of shapes are needed for the design of high-ohmic resistors, using existing technology layers. In case of high precision, the layout shape has to be taken into consideration.

A method for modelling of complex resistor layouts with elementary cells decomposition is proposed. The model has been investigated using the comparison between data for known shapes and test samples of non-typical shapes. The results reveal a good match with the model.

The model is easily applicable and very useful for demonstration of the layout influence upon resistors' parameters. Its usage will help the IC designers to gain experience needed for their professional tasks. Such kind of influence is noticed not only in resistor layouts but also in all layout elements.

11. REFERENCES

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