DIGITAL AUDIO PROGRAMMABLE TIME DELAY - AUDIO EFFECT

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The inclusion of programmable delay in low frequency audio signal has always been of interest in audio sound and recording. In this article an example of a schematic decision is presented to create a sound delay and level stabilizer. Additional programs and algorithms for cultivation of the audio signal are not included to the current problem. This project aims at the realization of a type of a programmable delay and stabilization of amplitude of the entrance audio signal with minimum harmonic distortion.

Keywords: audio, time delay, analog digital converter

1. TASK OF THE ARTICLE

Examining the group delay signal, we have to comply with the different delay in the various harmonious compositions. The inclusion of an echo in the audio signal denote grouping delay should not be smaller than $t_d = 50$ [ms].
There is no limit to the increase of this value but in practice it should not be larger than a few seconds. In the present article group programmable delay is limited to t_d=96 [ms]. For example sound delay depends of the volume of the sound and size of place.

Complete block schematic is shown on Fig.1.

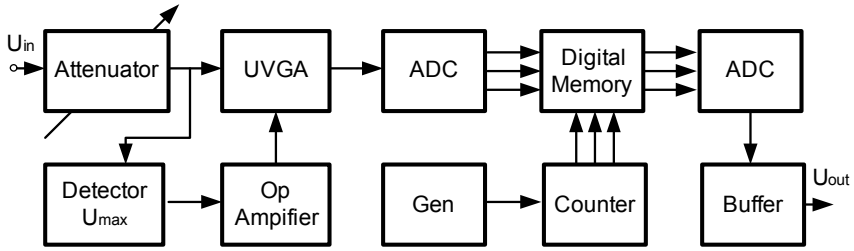

Fig.1. Bloc shematic

1.1. Amplitude limiter.

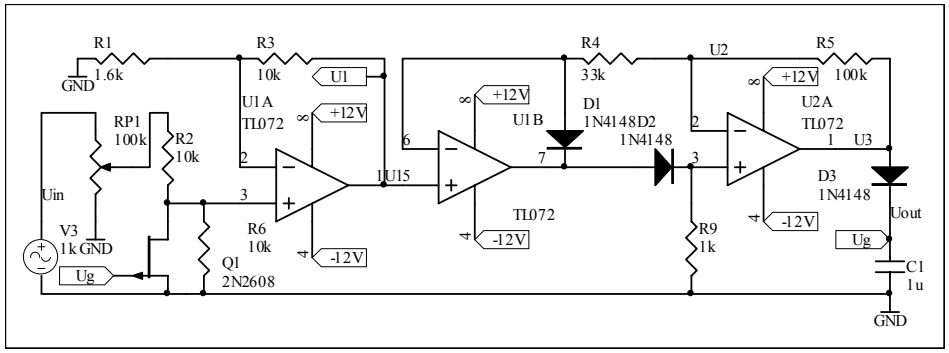

Fig.2. Amplitude stabilizer v.1.

As a practical way ti stabilize the amplitude of the input signal I use a chain of level correction which preserves the dynamics of the standard level of 0.775[V]. Which is kept constant within the whole frequency range change of the input – Fig.2. Variable resistor RP1 is used as an input chain of level regulation. Its function in the scheme is to set up (adjust) the input signal to the required standard limit. The value of the variable resistor has been chosen considering the Hi impedance of the input source (e.g. microphone, optical converter). Offer the variable resistor linking I have used the used a level separation group which consist of resistors R_2 and R_6. Their value has been chosen again having in mind the minimal loading of the input source. To this group, exactly, I attach field (JFET) transistor Q1 which I use as a regulated resistance. Its value os controlled by voltage Ug. In case that the output voltage has the standard level of U_{in} = 0.775 [V] the groups of the two serially circuited resistors R_2, R_6 and transistor Q1 reduces this level about 7 times. To compensate for this attenuation an additional amplification has been introduced and it is expressed by the equation:

$$(1)\ K_U = 1 + \frac{R_3}{R_1}$$

When we use the equivalent values of resistors R_2 and R_6 in formula.1 about the U1A amplification we get:

$$K_U = 1 + \frac{R_3}{R_1} = 1 + \frac{10.10^3}{1{,}6.10^3} = 1 + 6{,}25 = 7{,}25$$

In this way the signal receiving in the U1A output is transmitted to the entrance of a precise peak selector which consist of elements U1B, U2A, R4, R5, R9, D1, D2 и D3. The group represents a two half-period peak selector with high input impedance. Diode D3 attached to the exit provides the low pulsation of the output level with a very low value of capacitor C1. The voltage in this capacitor is used to control transistor Q1 and from there the value of the output voltage.

A considerably higher stability in the function of the limiter is achieved if we use a MOS instead of a field transistor– Fig.3.

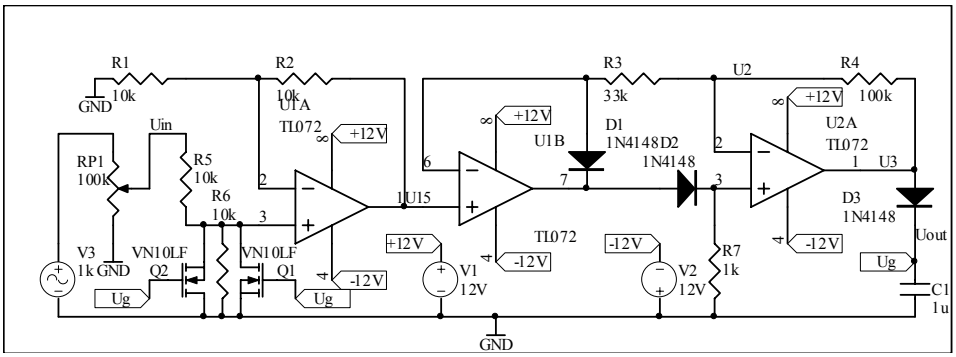

Fig.3. Amplitude stabilizer v.2.

A basic shortcoming of this linking is the appearance of non-linear deviation with input level of over 2V. To avoid this shortcoming correct the level through variable resistor RP1.

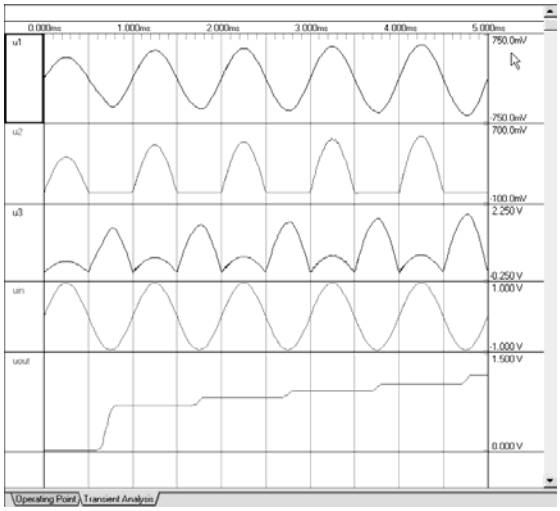

Fig.4.Simulation Result from Amplitude stabilizer v.1

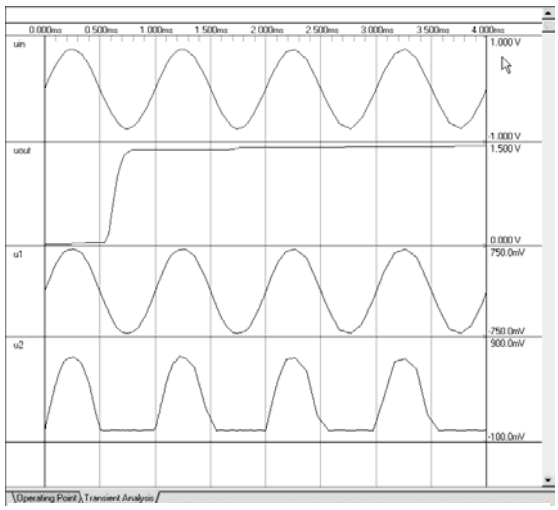

Fig.5.Simulation Result from Amplitude stabilizer v.2

The Received Simulation Result with programmed product Protel'99 is shown in Fig.4. "Simulation Result from Amplitude stabilizer v.1"; and Fig.5. "Simulation Result from Amplitude stabilizer v.2"

1.2. Audio digital delay line (ADDL).

To get a digital echo I use the method of splitting the input analogue signal into digital of transferring the information into an immediate memory which Brings about

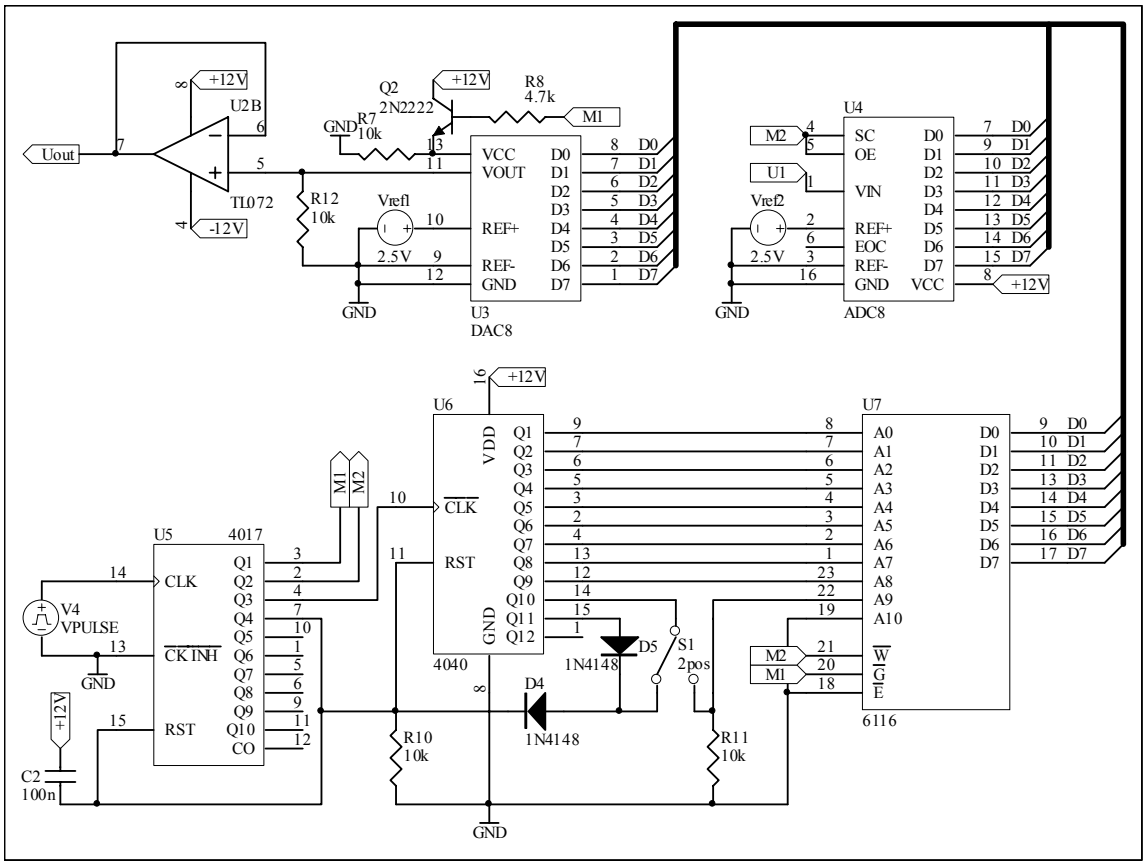

Fig.6. Audio digital delay line

the required delay and consequently converts the digital into analogue. The scheme in which the pointed order is shown in Fig.6. For the primary conversion of the analogue signal into digital an 8-bit digital analogue converter U4 has been used. In this way the digital signal received afterwards is simultaneously transmitted to the intermediate digital memory– U7 (1024x8) and to digital analog converter U3. The signal delay has been controlled by the method of successive reading and transcript from the memory while the encircling is always in the same direction. The digital addressing of the 8 bit memory has been alone with the help of counter U6. This is a 12-bit reveres counter which is linked as incomplete. The signal delay t_d depends on how many memory cells will be addressed counter U6 and is expressed by:

(2) $t_d = 2^n.t_{clk}$ [s]

where: t_{clk} – the period of input clock generator.

We use counting deciphering device U5 to control the successive cycle of reading and transcript in the memory. Its exits have been labeled Q1, Q2…Qn in turn. The first input impulse from V4 activates output Q1 of counter U5. In this way memory U7 can be read and digital analogue converter U3 is labeled and the digital word read from the memory is converted of the exit into analogue signal. With the second impulse of generator V4, output Q2 - counter U5 is labeled. Through net label M2 the same address is copied into the memory. The information recorded at that moment is used up by analogue digital converter U4. The third impulse of generator V4 – output Q3 is labeled and is a result changes the former of counter U7 into $Q^n=Q^{n+1}$. The next impulse of V4 puts Q5 in its off-position and activates output Q1.

Let's use "N" the number of the possible exit combination of U5. According to formula.2 the signal delay well be:

(3) $t_d = 2^n.N.t_{clk}$ [sec]

Example: the time of delay is t_d=24 [ms], N=3, n=10. Find the frequency of the time generator t_{clk}=?

According to formula.3, the value of t_{clk} is equal to:

$$t_{clk} = \frac{t_d}{2^n.N} = \frac{24.10^{-3}}{2^9.3} = 15{,}625.10^{-6} \text{ [sec] or } f_{clk} = \frac{1}{t_{clk}} = \frac{1}{15{,}625.10^{-6}} = 64.10^3 [Hz]$$

Similarly when we re-switch button S1 we get that the delay time is t_d=48 [ms].

Now let's consider the final version of this project.

1.3. The Complete Schematic.

The complete scheme of the project with delay time t_d=48 / 96 [ms] has been shown in Fig.7. The output sequence of the scheme is important, so an output buffer U2B is attached to amplify the current.

With this schematic layout in order to double the time of delay, the output digital word of counter U6 is changing by one bit. This also changes the time of delay t_d=48 / 96 [ms].

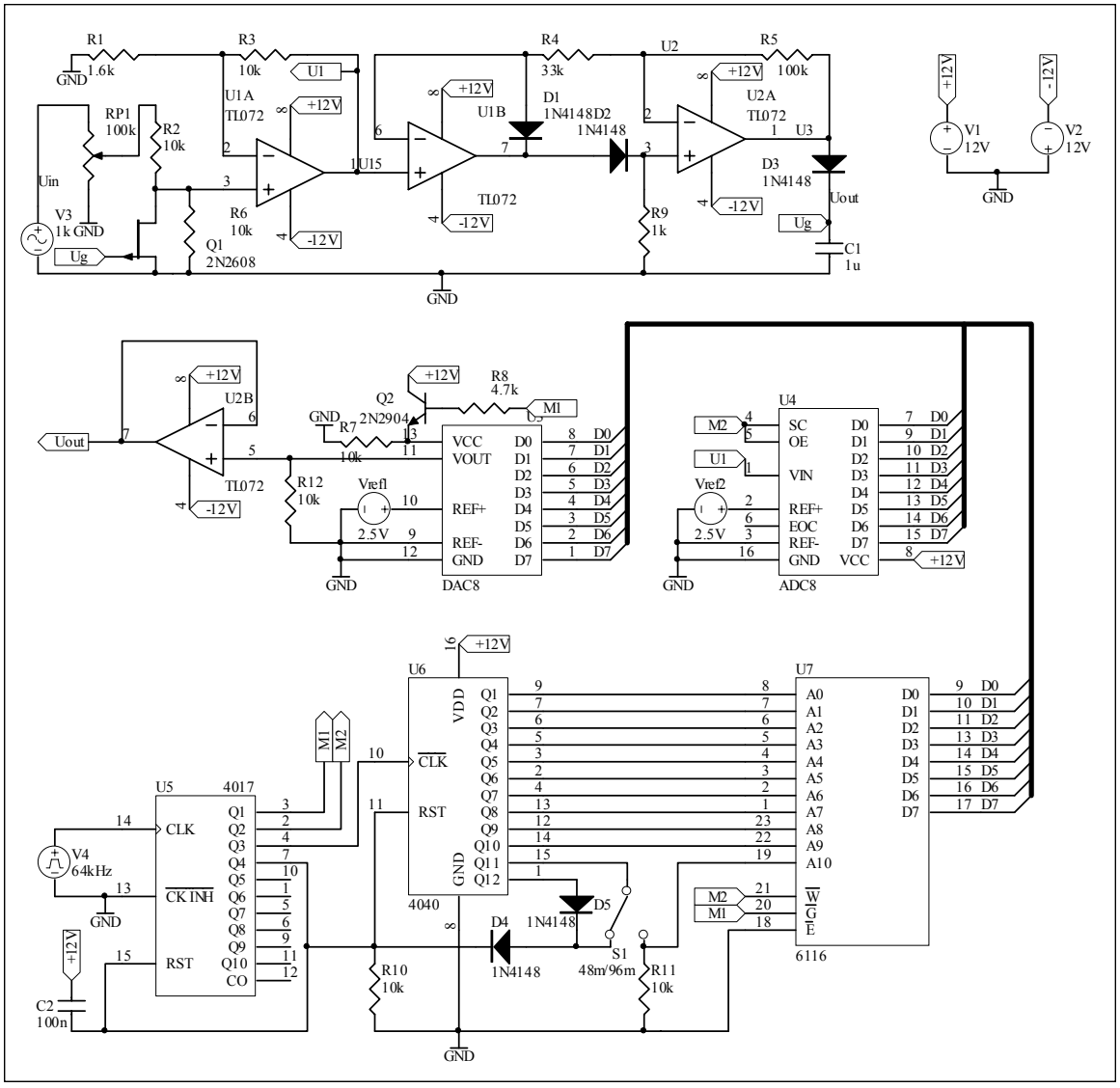

Fig.7. Complete schematic

The group C_2 and R_{10} is used as a beginning of the scheme. When we turn on the power supply for time $t=R_{10}.C_2$ [sec] we get a positive impulse which is transmitted is the reset entrance for the two integral schemes U5 and U6. When we cut the impulse and feed log.0. into the reser entrance we get a fixed pattern of counting. At the capacitor charget up to the power supply level. When we cut the power supply level we get a discharge on capacitor C_2 and a negative peak in resistor R_{10}. Diode D4 is used in order to protect the outputs of counter.

The function of the second diode D_{12} is to protect output Q_{12} of counter U6 while S1 is in the position shown in the scheme.

Simulation result of the equivalent signal delay according to the position of switch S1are show in Fig.8.

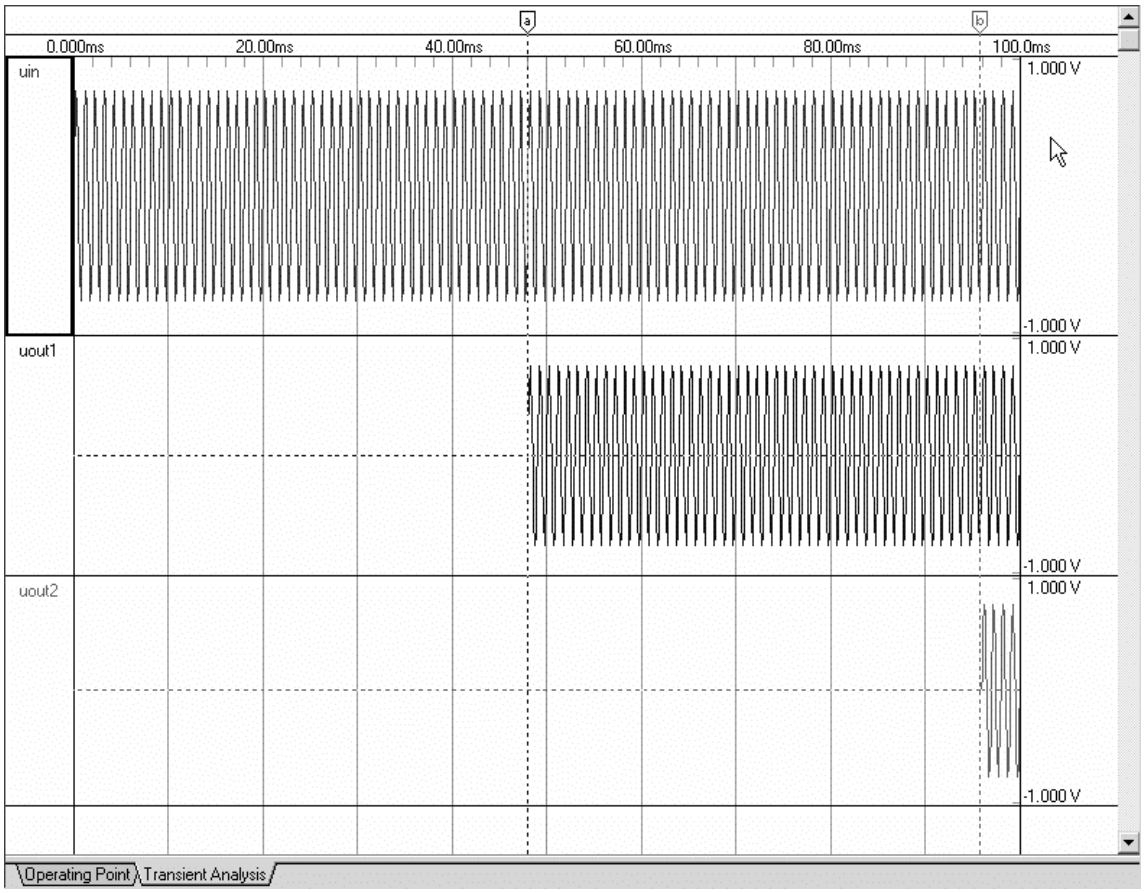

Fig.8. Compleate time delay

2. CONCLUSION

The present research suggests a practical way to achieve a programmed time delay. A system to suppress the output signal level has been introduced in order to limit the amplitude. This kind of stabilization does not produce a large harmonic distortion in the signal which makes if suitable for the Hi-Fi sound range. The enclosed simulation result show the principle of work and what has already been achieved By the project.

3. REFERENCES

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