# MONOLITHIC VOLTAGE-TO-FREQUENCY CONVERTERS MACROMODEL DEVELOPMENT

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*A macromodel of monolithic Voltage-to-Frequency Converter (VFC) for the simulator PSpice A/D is proposed. For creating the model, simplification and build-up techniques known from modelling operational amplifiers have been adapted. This generalized model is independent from actual technical realizations and is based upon compromises regarding the representation of exact circuit structure in the model. The proposed VFC model accurately predict the circuit behaviour for nonlinear dc, ac and large-signal transient responses. The macromodel topologies comprise of four stages: analogue integrator (input stage), comparator, one-shot timer and output delay stage. The equivalent circuit principally contains linear controlled sources, passive elements and voltage controlled switches. The SPICE diode and transistor models are used as non-linear elements for voltage limitation and approximation of characteristics. The macromodel is implemented as a hierarchical blocks and the structure of their netlist confirm to the standard SPICE format.*

**Keywords:** voltage-to-frequency converter, behavioural modelling, circuit simulation, SPICE.

## 1. INTRODUCTION

The monolithic Voltage-to-Frequency Converters (VFCs) are widely used in electronic circuits for analogue-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation and many other functions. The output signal of a VFC is pulse train at a frequency precisely proportional to the applied input voltage. Nowadays the analogue circuit design is perform using professional ECAD tools based on SPICE products. In order to decrease simulation time and convergence problems the last generation of SPICE simulators have introduced a new modelling technique the Analogue Behaviour Macromodelling (ABM) that consists in building a subcircuit description of the devices, using passive elements and controlled sources to implement the device's electrical characteristics [4]. The main advantages of the ABM method are the portability to all types of SPICE simulators and also the user's access to the macromodel's internal equations and variables. In [1] a behaviour macromodel of current-steering VCO is presented. The equivalent circuit of this model is based on the circuit introduced in [2] and contains analogue integrator presented as a controlled current source plus a capacitor and Schmitt trigger. Although this model provides ideal transfer function and useful simulation results, it is not present many first and second order effects of the real VFCs. More recently in [4], a square wave VCO model is presented. This macromodel with a suitable choice of parameters can be used of an analogue PLL circuit simulations, but not confirm to the architectures of a broad class of the monolithic VFCs. Without any doubt macromodels of VFCs

are necessary for simulating complex systems. However, powerful simulation models have not been available yet. This paper introduces a new behaviour model of monolithic charge balanced VFC.

## 2. FUNCTIONAL BLOCKS OF MODEL

The proposed macromodel of a charge balance VFC is developed following the design method based on a Top-Down analysis approach and applying simplification and build-up technique, known from modelling operational amplifiers [3]. The circuit diagram of the complete model is shown in Fig. 1, where the different stages are

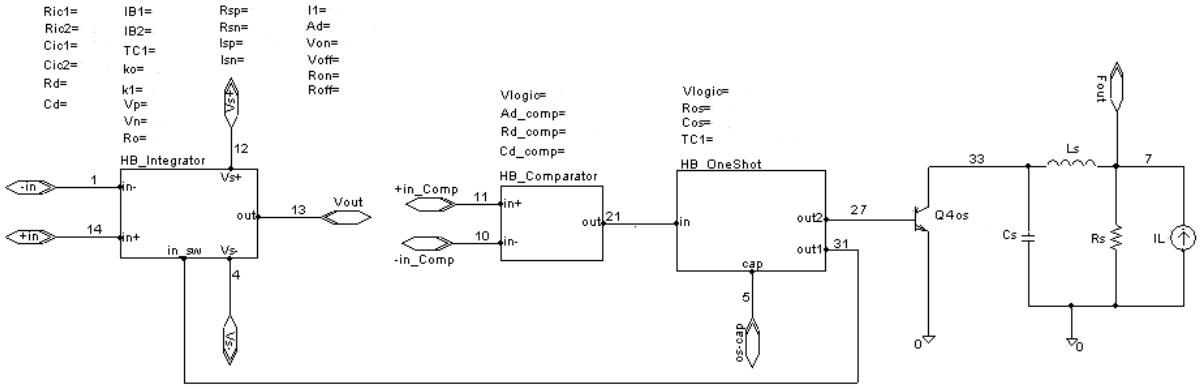


**Fig. 1.** Equivalent circuit of a VFC macromdoel

presented as a hierarchical blocks. The model parameters of the blocks are given without concrete numerical values. During the modelling of a particular IC the numerical values are obtained following the design procedure described further.

The entire model is divided into four functional blocks, each representing a subset of circuit parameters: analog integrator – input stage (HB_Integrator), voltage comparator (HB_Comparator), one-shot timer (HB_OneShot) and output delay stage. These functional blocks principally contain linear passive elements, controlled sources and ideal voltage controlled switches. The model has its own reference node which is different from the global reference node '0' in the PSpice simu-

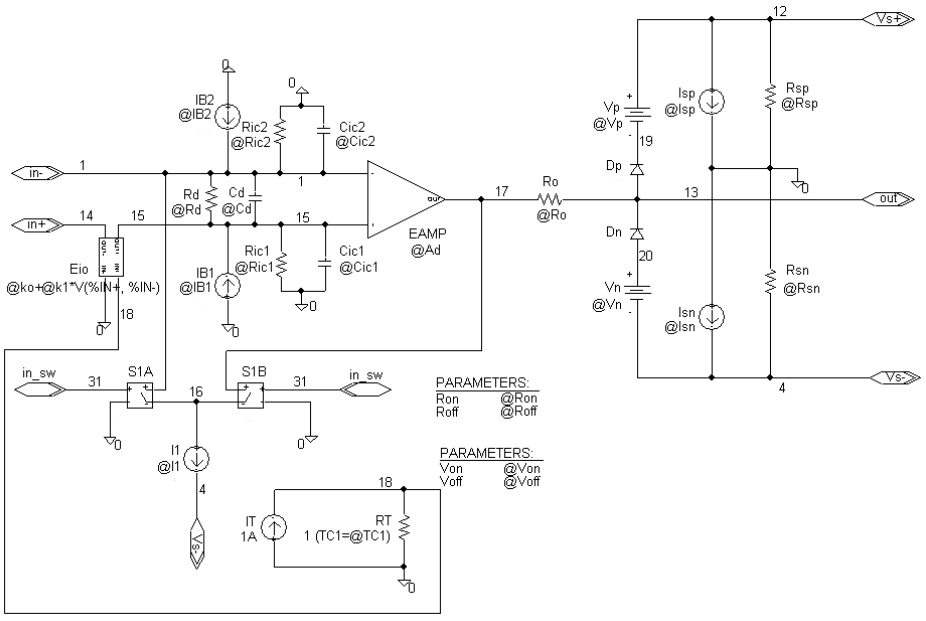


**Fig. 2.** Equivalent circuit of an input integrator – input stage (HB_Integrator)

lator for the purpose of implementing the model as a subcircuit into any arbitrary application circuit.

**2.1 Analogue integrator (input stage)**

The integrator stage, shown in Fig. 2 consists of two voltage-controlled voltage sources, eight ideal current and voltage sources, two voltage-controlled switches and several passive RC elements. The analogue integrator represents the parameters input impedance, bias and offset current, offset voltage and its temperature drift, voltage limitation, output resistance and supply current in a quiescent state. The ideal current source $I_1$ and voltage-controlled switches $S_{1A}$ and $S_{1B}$ correspond to the $I_{REF}$ and $S_1$ from the circuit presented in [6]. The resistance in "*ON"* and "*OFF"* mode of the switches are modelled with parameters $R_{on}$ and $R_{off}$, and the threshold voltages are simulated by $V_{on}$ and $V_{off}$. The switch parameters are defined in the equivalent circuit with additional elements '*param*'. The differential input resistance $R_{id}$ between inverting and non-inverting pins of the voltage source *EAMP* is produced by the elements $R_d$, $R_{ic1}$ and $R_{ic2}$.

(1) $R_{id} = R_d \,||\, (R_{ic1} + R_{ic2})$.

The common-mode input resistance $R_{icm}$ and capacitances $C_{icm}$ is provided by the elements $R_{ic1}$, $R_{ic2}$, $C_{ic1}$ and $C_{ic2}$.

(2a) $R_{icm} = R_{ic1} \,||\, R_{ic2}$, (2b) $C_{icm} = C_{ic1} + C_{ic2}$.

The bias current is generated by current sources $I_{B1}$ and $I_{B2}$ connected to node 1 and node 15, respectively. The input bias and offset current can be found by

(3a) $I_{iB} = (I_{B1} + I_{B2})/2$, (3b) $I_{iO} = I_{B1} - I_{B2}$.

The offset voltage $V_{iO}$ and its temperature drift for the macromodel is produced by the elements $E_{iO}$, $I_T$ and $R_T$. The temperature effects can be performed by appropriately selecting controlled voltages that are temperature dependent using the SPICE model of the temperature-dependent resistor.

(4a) $R(T) = R(TNOM)\left[1 + TC1(T - TNOM) + TC2(T - TNOM)^2\right]$

where $R(TNOM)$ is the value of the resistor at *TNOM* (usually $27°C$), $T$ is the temperature in $°C$, $TC1$ is the linear temperature coefficient and $TC2$ is the quadratic temperature coefficient. The equation (4a) will fit a quadratic curve through three points in a temperature graph by solving three equations with three unknowns. A sufficient degree of accuracy for the purpose of modelling offset voltage temperature drift has been provided by choosing $R_T$ as a linear temperature-dependent resistor ($TC2 = 0$) having the following characteristic equation:

(4b) $R(T) = R(TNOM)\left[1 + TC1(T - TNOM)\right]$.

The current source $I_T$ presents the voltage at node 18 that depends on the temperature drift. The generated current $I_T$ flow through the resistor $R_T$, towards the internal ground. In such a way the voltage $u_{18}$ will depend upon the temperature.

(5) $u_{18} = I_T R_T \left[1 + TC1(T - TNOM)\right]$.

The parameters of the current $I_T$ and the resistor $R_T$ are extracted such that the temperature stage provides a voltage $u_{18} = 1V$ at the temperature $TNOM$. Signal generated at nodes 18 are used for forming the characteristic equation of $E_{iO}$ as follows:

(6) $u(E_{iO}) = k_{o,E_{iO}} + k_{1,E_{iO}} u_{18} = k_{o,E_{iO}} + k_{1,E_{iO}} \{I_T R_T [1 + TC1(T - TNOM)]\} = V_{iO} + \alpha_{V_{iO}} \Delta T$

where the offset voltage $V_{iO}$ at $T = TNOM$ is determined by

(7) $V_{iO} = k_{o,E_{iO}} + k_{1,E_{iO}} I_T R_T$ and the temperature coefficient $\alpha_{V_{iO}}$ of the input offset voltage is calculated from

(8) $\alpha_{V_{iO}} = k_{1,E_{os}} TC1(I_T R_T)$.

There are two equations, (7) and (8), for determining the coefficients $k_{o,E_{iO}}$, $k_{1,E_{iO}}$ and $TC1$. The differential mode voltage gain is provided by the voltage-controlled voltage source *EAMP*. This voltage source with its gain $A_d$ is controlled by the differential input voltage $V_{15,1}$. In principally the value of $A_d = 1000$ is chosen arbitrary, because the input stage operating as an ideal integrator. The voltage-clamp circuit produced the desired maximum voltage excursion with two diodes ($D_p - D_n$) each in series with a voltage source ($V_p - V_n$). The clamping circuit prevent node 13 from reaching several thousands of volts which could cause convergence problems during simulation. The positive output voltage is clamped by $D_p$ and cannot exceed

(9a) $V_{O\max p} = V_{Sp} - V_p - V_{D_p} = V_{Sp} - V_p + V_T \, ln(I_{O\max p} / I_{SD_p})$.

In same manner, the negative output voltage is limited by

(9b) $V_{O\max n} = V_{Sn} - V_n - V_{D_n} = V_{Sn} - V_n + V_T \, ln(I_{O\max n} / I_{SD_n})$

where $I_{SD_P}$ and $I_{SD_n}$ are saturation current of diodes $D_p$ and $D_n$, $I_{O\max p}$ and $I_{O\max n}$ is maximum current through diodes and $V_T$ is the thermal voltage.

Quiescent current is modelled with the combination of $I_{Sp}$ ($I_{Sn}$) and the $R_{Sp} - R_{Sn}$ series resistors. As the supply voltage increases, the current through $R_{Sp}$ and $R_{Sn}$ will increase effectively simulating that behaviour in the real devices. The total supply currents from positive and negative rails at a given voltage $V_{Sp}$ ($V_{Sn}$) are

(10a) $I_S^+ = I_{Sp} + V_{Sp} / R_{Sp}$ and (10b) $I_S^- = I_{Sn} + V_{Sn} / R_{Sn} + I_1$.

The output resistance of the integrator is modelled by the resistor $R_o$ connected between nodes 17 and 13.

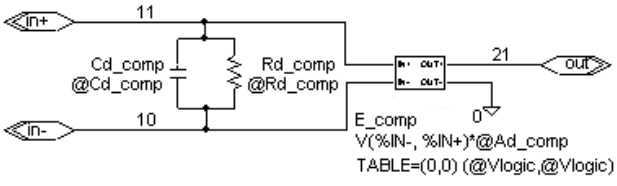


**Fig. 3.** Equivalent circuit of a voltage comparator (HB_Comparator)

## 2.2 Voltage comparator (second stage)

The second stage of the macromodel provides the parameters input resistance, input capacitance and logic levels of the comparator output voltage. Figure 3 illustrates the functional block model of

the comparator for a symmetric input, which is also intended for modelling an asymmetrical input with an external reference voltage source connected at node 11. Voltage source $E_{comp}$ is controlled by the differential voltage between nodes 11 and 10, and its gain $A_{d\_comp}$ is set greater than unity for simplify. The output logic levels $V_{S\_neg}$ and $V_{S\_pos}$ of the model is defined in the TABLE parameter of $E_{comp}$. The differential input impedance of the comparator is modelled with the combination of resistor $R_{d\_comp}$ and capacitor $C_{d\_comp}$.

### 2.3 One shot timer (third stage)

The one shot timer block of the macromodel, shown in Fig. 4 performs three important functions, namely, simulation of one shot time period, operating frequency range and output frequency versus temperature. The functional block consists of an RS flip-flop ($U_{1A}$ and $U_{2A}$) and a timer comparator presented with ideal voltage sources $E_{os1}$ and $E_{os2}$. The BUFST1 and BUFST2 Schmitt-trigger buffers connected between analogue outputs and digital inputs prevents analogue voltages that transition through the digital dead zone from even temporarily affecting the digital inputs. The Schmitt-trigger buffers are based on the 7414 gates [5]. The supply

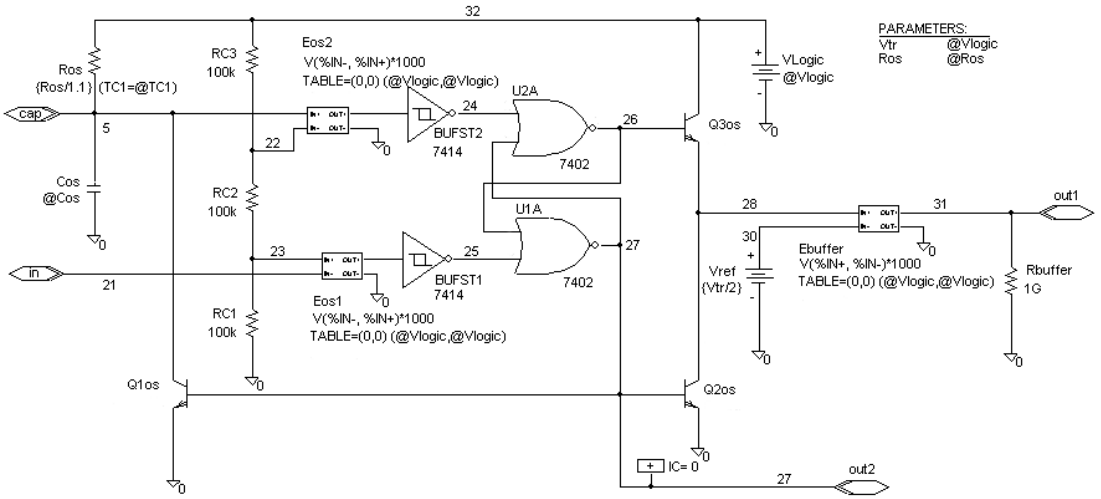


**Fig. 4.** Equivalent circuit of an one shot timer (HB_OneShot)

voltage of this stage is provided with the voltage source $V_{log\,ic} = +5V$ connected to node 32. The output voltage of the timer block at node 31 is generated by voltage-controlled voltage source $E_{buffer}$. The resistor $R_{buffer}$ provides a DC path to node 31 as required in SPICE and is set to $1G\Omega$.

The function of the comparator (HB_Comparator) is to compare the positive input voltage at node 11 to the voltage at node 10. If the voltage at noninverting input is smaller, the comparator will trigger the one shot timer. The output voltages of the timer (nodes 31 and 27) will turn *OFF* both the output transistor $Q_{1os}$ and the voltage-controlled switch $S_{B1}$ (from the input stage) for a time period

(11a) $t_{os} = 1{,}1R_{os}\left(C_1 + C_{os}\right)$

where $C_1$ is an external capacitor and $C_{os}R_{os}$ network define the maximum output frequency. The value of resistor $R_{os}$ is defined in the equivalent circuit with additional element '*param*'.

The one shot time period depend linearly on external timing capacitor $C_1$. When $C_1 = 0$ the following approximate expression can be written for the minimum time period

(11b) $t_{os\min} = 1{,}1R_{os}C_{os}$.

The predominant thermal effect of a voltage-to-frequency converter is the change in output frequency as a function of temperature. For the macromodel the temperature drift is produced by the linear temperature-dependent resistor $R_{os}$ connected between nodes 32 and 5.

(12) $$f_{out} = \frac{I_{in}}{I_1(C_1 + C_{os})R(TNOM)[1 + TC1(T - TNOM)]}.$$

The temperature drift of the output frequency is determined by

(13) $$\delta_{fT} = \frac{\Delta f_{out}}{f_{out}} = 1 - \frac{1 + TC1(T_{min} - TNOM)}{1 + TC1(T_{max} - TNOM)}$$ where $T_{min}$ and $T_{max}$ are the minimum and maximum temperature of the operating range.

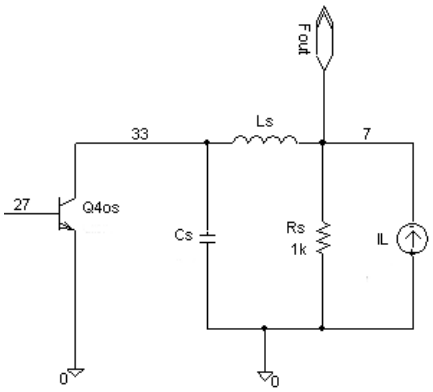


**Fig. 5.** Equivalent circuit of an output stage

### 2.4 Output stage

The output stage models peak overshoot factor, rise time and settling time of the output waveform. This functional block (Fig. 5) consists of an ideal inverter and a second-order output delay stage. The output voltage inverter is contains of an ideal transistor $Q_{4os}$ with open collector. The inverter is intended for modelling the logic levels of the output voltage referred to node 7 of the model. When the transistor $Q_{4os}$ is "OFF" (logic level "1") the voltage generated at node 7 can be found by

(14) $$u_7 = R_s(I_L + I_{Leakage})$$

where $I_{Leakage}$ is the output leakage current in a logic level "1" and $I_L$ is the reference current generated by the ideal source connected in parallel of the resistor $R_s$.

The inverse Laplace transform of the delay stage function provides the voltage $u_7$ in the time domain.

(15) $$u_7(t) = \left[1 + \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_o t} \sin\left(\omega_o\sqrt{1-\xi^2}\,t + \varphi\right)\right](R_s \,||\, R_2)I_{33}$$ where

(16) $$\varphi = acr\,tan\left(\sqrt{1-\xi^2}\,/\,\xi\right)$$

(17a) $\omega_o = (L_s C_s)^{-\frac{1}{2}}$ is the resonant frequency,

(17b) $\xi = \frac{R_s \parallel R_2}{2}\sqrt{\frac{C_s}{L_s}}$ is the damping ratio and $R_2$ is the external pull-up resistor connected to the logic supply voltage.

For $0 < \xi < 1$, $u_7$ it seen to overshoot and settle to the steady-state value in an oscillation manner. The first extreme of the step response (15) provides the peak overshoot (maximum). To determine the time of the peak overshoot, is set the derivative $du_7(t)/dt = 0$ and solve for $t = t_p$ of the first peak, i.e.

(18) $t_p = \pi / \omega_o \sqrt{1-\xi^2}$.

Substituting Eq. (18) back into Eq. (15) for *t*, is obtained the value for the peak overshoot $u_{7\max}$, i.e.

(19) $u_{7\max} = u_7(t_p) = \left(1 + e^{-\pi\xi/\sqrt{1-\xi^2}}\right)(R_s \parallel R_2)I_{33}$.

The settling time $t_s$ is defined by the time instant where the enveloping curve reaches the relative deviation $\varepsilon$ ($\varepsilon = 0{,}01$ or $\varepsilon = 0{,}001$) from the final or steady-state value of the output.

(20) $$t_s(\varepsilon) = 2\pi(R_s \parallel R_2)C_s\left\{\frac{2\cos(PM)}{\sin^2(PM)}\left[\ln(\varepsilon) + \frac{1}{2}\ln\left(1 - \frac{\sin^2(PM)}{4\cos(PM)}\right)\right]\right\}$$

where $PM = \arccos\left[\sqrt{1+4\xi^2} - 2\xi^2\right]$.

With the resistor $R_s$ set to $1k\Omega$, the three parameters $L_s$, $C_s$ and $I_L$ can be determined if the peak overshot factor, the settling time and the steady-state value of the output waveform are given.

## 3. CONCLUSIONS

In this paper a behaviour macromodel of voltage-to-frequency converters for the simulator SPICE based on the data sheet electrical characteristics has been presented. The proposed model allows simulating arbitrary user circuits with respect to the behaviour in both time and frequency domains, including effects such as accurate input transfer characteristic, accurate transient response, temperature dependence of several parameters, input impedance and voltage limitation. The model is not capable of simulating PSRR, noise, parasitic effects of device package, parametric variation, etc.

## 4. REFERENCES

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