DESIGN PROCEDURE AND VALIDATION OF A VFC MACROMODEL

Ivailo Milanov Pandiev

Department of Electronics, Technical University of Sofia, Kliment Ohridski Street No 8, 1000 Sofia, Bulgaria, phone: +359 2 965 2620, e-mail: ipandiev@tu-sofia.bg

A systematic approach for designing a VFC behaviour macromodel is presented. The design method of the macromodel suggested can be split into two basic steps: 1) model parameter extraction using typical values of the data sheet parameters; 2) verification (or debugging) of the proposed model. Model parameters are extracted for the integrated voltage-to-frequency converter ADVFC32 from Analog Devices as an example. To confirm the validity of the model, simulation results are compared with the manufacturer's data, where is found good agreement between simulations and performance of the actual devices.

Keywords: voltage-to-frequency converter, behavioural modelling, verification, circuit simulation, PSpice

1. VFC MACROMODEL DESIGN PROCEDURE

The design method of the VFC macromodel [1] in this paper can be split into two steps. The first step consists of the suitable selection of the parameters and elements of the equivalent circuit from data sheet parameters. The advantage of this approach is that parameter extraction can be performed only from data sheet parameters, even for circuits whose internal structure is unknown. In developing a macromodel, a real device is measured in terms of lab and data sheet performance, and the macromodel is adjusted to match this behaviour. The second step comprises the verification of the proposed model. The verification checks are implemented within EDA OrCAD following the test conditions given in the manufacture's data. During the process of verification, an investigation of each element or functional block (group of elements) in the model is performed. Each element of the equivalent circuit is tested in turn to ensure that, firstly, it behaves in the manner intended by the model description (model code) and secondly, that its behaviour correspond to the operation of the real integrated circuit.

In this section, expressions are developed to relate the performance of the VFC and the macromodel to the parameters and elements of the equivalent circuit. A summery of all design equations are given in Table I. The parameters extraction of the model proceeds from the input, transfer and output characteristics of the VFC.

Table I. Design equations for the VFC macromodel

$V_T = kT/q = 25{,}85mV$ for $300K$	$R_{S_p} = R_{S_n} = \Delta V_{CC} / \Delta I_S^+ = \Delta V_{EE} / \Delta I_S^-$ **(1)**
$I_{SD_p} = I_{SD_n} = 8.10^{-16} A$	$I_{Sp} = I_{Sp}^+ - \dfrac{V_{Sp}}{R_{Sp}}$
$R_{ic1} = R_{ic2} = 2R_{icm}$	$I_1 = \dfrac{I_{inFS}}{f_{outFS}.t_{os\min}}$ **(2)**

$C_{ic1} = C_{ic2} = C_{icm} / 2$	$I_{Sn} = I_{Sn}^{-} - \frac{V_{Sn}}{R_{Sn}} - I_1$
$R_d = \frac{R_{id}\left(R_{ic1} + R_{ic2}\right)}{R_{ic1} + R_{ic2} - R_{id}}$ $C_d = C_{id} - C_{ic1} = C_{id} - C_{ic2}$ $I_{B1} = I_{iB} + \frac{I_{iO}}{2}$ $I_{B2} = I_{iB} - \frac{I_{iO}}{2}$ $TC1 \le \frac{10^{-1}}{TNOM - T_{min}}$ of R_T **(3)** $k_{1,E_{iO}} = \frac{\alpha_{U_{iO}}}{TC1\left(I_T R_T\right)}$ **(4)** $k_{o,E_{iO}} = V_{iO} - k_{1,E_{iO}}$ $R_o = R_{out}$ $V_p = V_{Sp} - V_{O\max p} + V_T \ln \frac{I_{O\max p}}{I_{SD_p}}$ $V_n = V_{Sn} - V_{O\max n} + V_T \ln \frac{I_{O\max n}}{I_{SD_n}}$	$R_{d\_comp} = R_d$, $C_{d\_comp} = C_d$ for comparator $R_{C1} = R_{C2} = R_{C3} = 1k\Omega$ $C_{os} = \frac{t_{os\,min}}{1{,}1R\left(TNOM\right)}$ **(5)** $TC1 = \frac{\delta_{f_T}}{\left(1 - \delta_{f_T}\right)\left(T_{max} - TNOM\right) - \left(T_{min} - TNOM\right)}$ of R_{os} $\xi = -\frac{ln\left(\delta_{os} - 1\right)}{\sqrt{\pi^2 + \left[ln\left(\delta_{os} - 1\right)\right]^2}}$ **(6)** $C_s = \frac{t_s(\varepsilon)}{2\pi\left(R_s \,||\, R_2\right)\left\{\frac{2\cos(PM)}{\sin^2(PM)}\left[ln(\varepsilon) + \frac{1}{2}ln\left(1 - \frac{\sin^2(PM)}{4\cos(PM)}\right)\right]\right\}}$ **(7)** $PM = arccos\left[\sqrt{1 + 4\xi^2} - 2\xi^2\right]$ $L_s = C_s\left(\frac{R_s \,||\, R_2}{2\xi}\right)^2$ $I_L = \frac{V_{7\,max}}{R_{os}} - 2I_{Leakage}$

Notes:

(1) $\Delta V_{Sp} / \Delta I_{Sp}^{+}, \Delta V_{Sn} / \Delta I_{Sn}^{-}$ is the change in supply voltage by the change in supply current anywhere within the operating range of the VFC;

(2) f_{outFS} is a full scale frequency corresponding to maximum input current $I_{inFS} = V_{inFS} / R_{in}$ and $t_{os\,\min}$ is minimum one shot time period;

(3) $T_{\min}$ is the minimum temperature in the operating range of the VFC;

(4) The resistor R_T is set to 1Ω. The low value is chosen to minimize the thermal noise associated with this resistor and to simplify the calculations for the other components in the stage. According to equation (5) introduced in [1] current source is fixed at $1A$ to provides a voltage $u_{18} = 1V$ at the temperature $TNOM = 27°C$;

(5) $R\left(TNOM\right)$ is the value of the resistor R_{os} at room temperature ($TNOM = 27°C$) and the value of temperature-dependent resistor R_{os} is obtained from the specifications for the minimum one shot time period $t_{os\,\min}$ and temperature drift of the output frequency δ_{f_T};

(6) $\delta_{os} = V_{7max} / V_s$ (V_{7max} - maximum output voltage at $t = t_p$, V_s - steady-state value of the output voltage) is the overshoot factor of the output voltage;

(7) The external pull-up resistance R_2 is chosen with default value of $1k\Omega$ and relative deviation ε is within 1% or 0,1%;

2. MODEL OF VOLTAGE-TO-FREQUENCY CONVERTER ADVFC32

In this section, an example is used to illustrate the design procedure of the VFC macromodel. A model for ADVFC32 has been build and tested within OrCAD. The ADVFC32 is a monolithic charge-balance voltage-to-frequency converter (or frequency-to-voltage converter) with operating frequency up to $0{,}5MHz$ [3]. The development procedure of the macromodel follows the sequence of expressions of Table I. The final results are presented in Table II.

Table II. ADVFC32 model parameters

Parameter	Value	Unit	Parameter	Value	Unit
T	300	K	$R_{S_p} = R_{S_n}$	150	$k\Omega$
$I_{SD_p} = I_{SD_n}$	8.10^{-16}	A	I_{Sp}	4,94	mA
R_{ic1}	1,5	$10^9\Omega$	I_{Sn}	3,94	mA
R_{ic2}	1,5	$10^9\Omega$	I_1	1	mA
C_{ic1}	1,5	pF	V_{s_neg}	0	V
C_{ic2}	1,5	pF	V_{s_pos}	5	V
R_d	2	$M\Omega$	R_{d_comp}	250	$k\Omega$
C_d	8,5	pF	C_{d_comp}	10	pF
I_{B1}	40	nA	$R_{C1} = R_{C2} = R_{C3}$	100	$k\Omega$
I_{B2}	8	nA	C_{os}	44	pF
$TC1$ of R_T	0,001	$°C^{-1}$	$TC1$ of R_{os}	37,621325	$10^{-6}°C^{-1}$
$k_{1,E_{iO}}$	30	mV	ξ	0,8	-
$k_{o,E_{iO}}$	-26	mV	C_s	50	pF
V_p	5	V	L_s	4,8828	μH
V_n	5	V	R_s	1	$k\Omega$
R_o	50	Ω	I_L	4,998	mA

3. MACROMODEL VALIDATION

A validation check of the new macromodel is performed by comparison analysis between simulation results and physical test of the VFC circuit ADVFC32KN for different types of feedback and timing capacitor connections. The simulation mo-

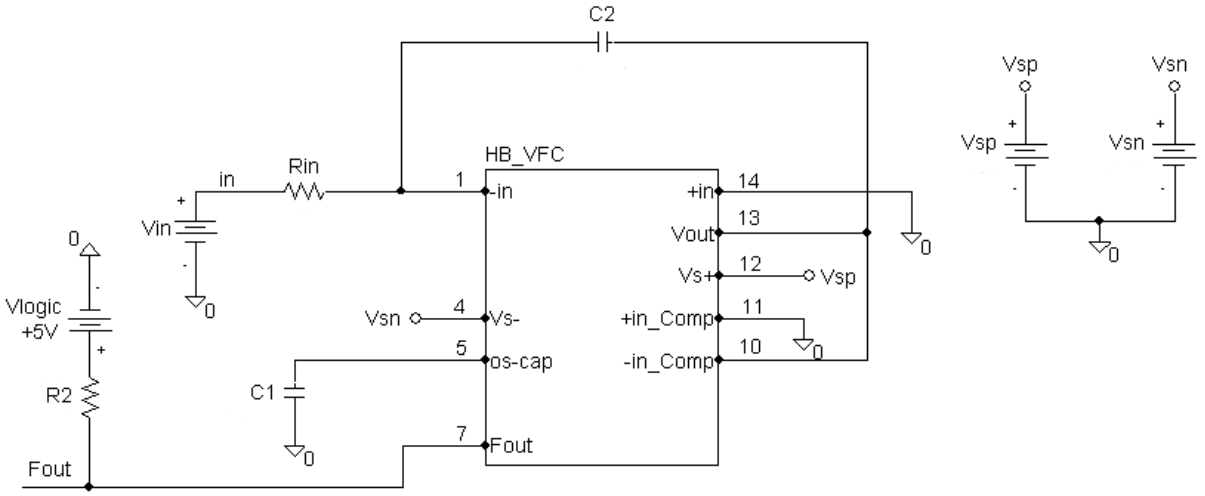
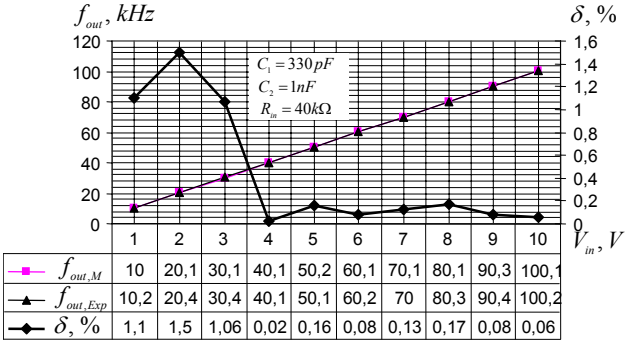


Fig. 1. Test circuit for simulation

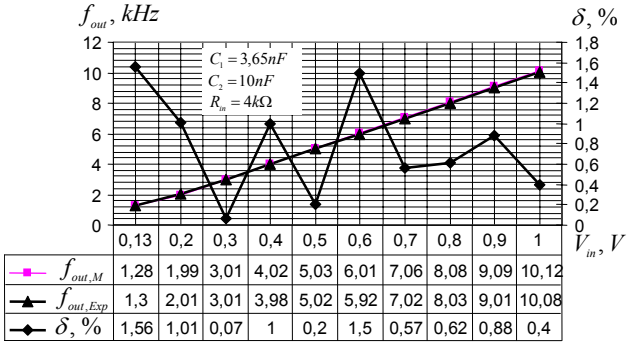
delling is implemented within EDA OrCAD. During the process of simulations are specified and performed parametric dc, ac and transient analyses. The global parameters are dc input voltage, operating temperature and various types of feedback. The test circuit for simulation is shown in Fig. 1, where the model of VFC (HB_VFC) is presented as a structure of hierarchical blocks. To associate the model block with the entire circuit diagrams the same node numbers as in Fig. 1 from paper [1] are used.

During the physical experiments the shape, amplitude and frequency of the signals at nodes 7, 13 and 5 are measured. The supply voltage for the circuit is chosen $\pm 15V$. In the Fig. 2a and Fig. 2b are presented simulation output, experimental results for the output frequency f_{out} and error in percents ($\delta = \left[\left(f_{,out,M} - f_{,out,Exp}\right)/ f_{,out,M}\right]100\%$) at $C_1 = 330\,pF$ ($R_{in} = 40k\Omega$, $C_2 = 1nF$) and $C_1 = 3{,}65nF$ ($R_{in} = 4k\Omega$, $C_2 = 10nF$) versus V_{in}. The pull-up resistor R_2 is set to $1k\Omega$. In the tables below (Fig. 2a and Fig. 2b) are given numerical values for the VFC



	1	2	3	4	5	6	7	8	9	10
$f_{out,M}$	10	20,1	30,1	40,1	50,2	60,1	70,1	80,1	90,3	100,1
$f_{out,Exp}$	10,2	20,4	30,4	40,1	50,1	60,2	70	80,3	90,4	100,2
δ, %	1,1	1,5	1,06	0,02	0,16	0,08	0,13	0,17	0,08	0,06

Fig. 2a. Comparison of the model and experimental results for f_{out} at $C_1 = 330\,pF$



	0,13	0,2	0,3	0,4	0,5	0,6	0,7	0,8	0,9	1
$f_{out,M}$	1,28	1,99	3,01	4,02	5,03	6,01	7,06	8,08	9,09	10,12
$f_{out,Exp}$	1,3	2,01	3,01	3,98	5,02	5,92	7,02	8,03	9,01	10,08
δ, %	1,56	1,01	0,07	1	0,2	1,5	0,57	0,62	0,88	0,4

Fig. 2b. Comparison of the model and experimental results for f_{out} at $C_1 = 3{,}65nF$

parameters, simulation results and errors. Notice that the simulated parameters closely match of the actual device ($\delta < 2\%$). The model performance characteristics are listed in Table III in comparison with the measured data of the real IC. As can be seen, the goal of a 5% match between the macromodel and the actual device was achieved, which guarantee the correct degree of accuracy.

Table III. Comparison between simulation results and data sheet parameters

Parameter	Symbol	Conditions	Data sheet			Model	Unit
			Min.	Typ.	Max.		
Dynamic performance							
Frequency range	$f_{out,\max}$		0		500	0 - 550	*kHz*
vs. Temperature	δ_{f_T}	$T_{\min} - T_{\max}$		75		71,57	*ppm / °C*
Rise time	t_r	$V_{in} = 10V$ $V_{in} = 1V$		35 35		35,5 35,5	*ns* *ns*
Settling time	t_s	$V_{in} = 10V$, $\varepsilon = 1\%$ $V_{in} = 1V$, $\varepsilon = 1\%$		150 150		151 152	*ns* *ns*
Overshoot factor	δ_{os}	$V_{in} = 1V$, $C_1 = 3{,}65nF$		1,015		1,016	-
Analogue input integrator							
Input offset voltage	V_{iO}	$T_A = 25°C$			4	4,001	*mV*
vs. Temperature	$\alpha_{V_{iO}}$	$T_{\min} - T_{\max}$			30	30,1	$\mu V / °C$
Input bias current	I_{iB}	$T_A = 25°C$		24		24	*nA*
Input offset current	I_{iO}	$T_A = 25°C$		32		32	*nA*
Differential Resistance	R_{id}			2		2	$M\Omega$
Diff. Capacitance	C_{id}			10		10	*pF*
Common-mode Res.	R_{ic}			750		750	$M\Omega$
Common-mode Cap.	C_{ic}		3			3	*pF*
Voltage Input Range	$V_{O\max p,n}$	$V_{Sp,n} = \pm 15V$	0		10	10	*V*
Output resistance	R_{out}			50		50	Ω
Comparator							
Logic "0" Level	V_L		$-V_S$		-0,6	0	*V*
Logic "1" Level	V_H		1		$+V_S$	15	*V*
Pulse Width Range	$t_{os\min}$	$I_{inFS} = 0{,}25mA$, $f_{out,\max} = 500kHz$			300	306	*ns*
Differential Resistance	R_{id}			250		250	$k\Omega$
Diff. Capacitance	C_{id}		10			10	*pF*
Open collector output							
Output voltage	V_{oL}	Logic "0"			0,04	0,04	*V*
Output voltage	V_{oH}	Logic "1"			5	4,9	*V*
Output leakage current	I_L	Logic "1"			1	1	μA
Supply characteristics							
Quiescent current	$I_{Sp,n}$	$V_{Sp,n} = \pm 15V$ $V_{Sp,n} = \pm 9V$		5,04 5,00		5,038 5,00	*mA* *mA*
Supply current drift	δ_{Is}			6,67		6,33	$\mu A / V$

4. CONCLUSIONS

In this paper a systematic procedure to design a behaviour VFC macromodel has been presented. The advantage of this method is that parameter extraction can be performed only from manufacture's data, even for circuits whose internal structure is unknown. The efficiency of the VFC model was proved by comparison of simulation results and data sheet parameters of the monolithic voltage-to-frequency converter ADVFC32 from Analog Devices.

5. REFERENCES

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