HIGH VOLTAGE MODULE FOR THE PHOTOMULTIPLIER POWER SUPPLY SYSTEM OF THE CMS FORWARD HADRON CALORIMETER

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Quartz fibers operating as Cherenkov detectors are used in the CMS Forward Hadron Calorimeter and about 1700 photomultiplyers (PMTs) transform their light pulses in electrical signals. A very economical high voltage power supply system is designed in which up to 72 PMTs are supplied by 3 HV channels. In this way the whole system consists only of 8 high voltage power supply modules (HV modules) housed in 2 Eurocrates. Each HV module contains three clusters (A, B, C) of three channels. The channels of each cluster generate different high voltages: first channel (A1, B1, C1) – up to 2000 V; second channel (A2, B2, C2) – up to 800 V; third channel (A3, B3, C3) – up to 400 V. All channels are fully computer controlled through a crate controller and a local module control block. The internal structure and the operation of the HV module are described.

Keywords: calorimeter, Cherenkov detector, high voltage, photomultiplyer.

1. INTRODUCTION

Quartz fibers operating as Cherenkov detectors are used in the CMS Forward Hadron Calorimeter (HF), where 1728 photomultiplyer tubes (PMTs) transform their light pulses in electrical signals [1]. A very economic high voltage power supply system is designed in which groups of 72 PMTs are supplied by only three HV channels [2]. For this purpose each 8 PMTs are mounted on one printed circuit board (fig. 1) using 3 supply voltages: U_K – feeding a resistive divider for the cathode and the first 6 dynodes of all 8 PMTs; U_{D7} – supplying their seventh dynodes (D_7); U_{D8} – supplying the eighth dynodes (D_8). Nine PCBs of this type (i.e. 72 PMTs) are supplied by one cluster of 3 HV channels.

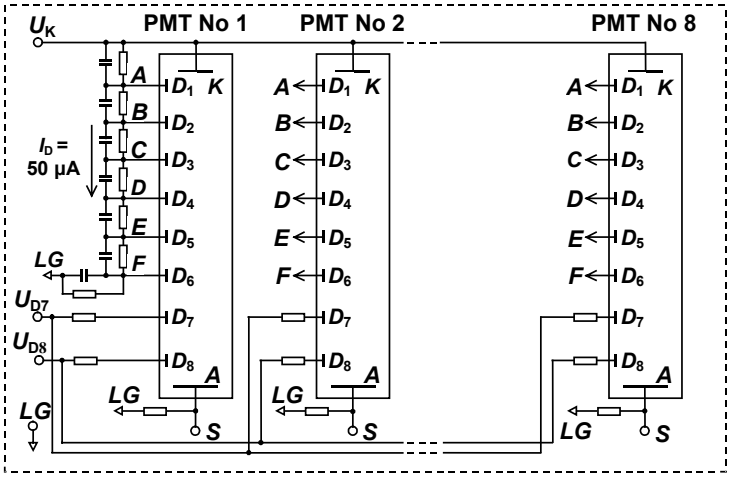

Fig. 1. Block diagram of the photomultiplier's PCB.

In this way only 24 clusters of 3 HV channels are required for the whole photomultiplyer power supply system. Three clusters (i.e. 9 channels) are installed in one

HV module. Thus whole system will consists of 8 modules, which are housed in two Eurocrates together with one Crate controller module in each of them [3].

2. HIGH VOLTAGE POWER SUPPLY MODULE

2.1. Internal structure and operation

The block diagram of the HV module is shown in fig. 2. As mentioned above it contains 3 clusters (A, B and C) of 3 channels. The output voltage of first channel in each cluster (A1, B1 and C1) is intended to supply the PMTs resistive dividers (see fig. 1) and can be regulated from 0 to −2000 V. The second channel produces the voltage for the D_7 dynodes and can be vary from 0 to −800 V. The third channel generates the D_8 voltage – from 0 to −400 V.

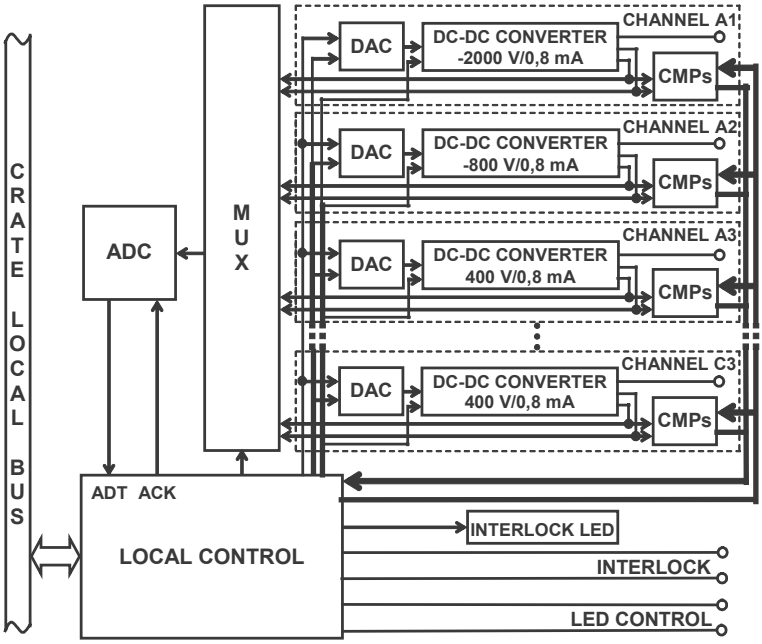

Fig. 2. Block diagram of the HV module.

Each high voltage channel includes one 12-bit serial digital-to-analog converter (DAC), a DC-DC converter (see Sect. 2.2) and two comparators (CMPs) for overvoltage and overcurrent protection.

A LOCAL CONTROL block (see Sect. 2.3) receives all output voltage set values sent in serial mode by the crate controller via the "crate local bus". These set values are then transferred and stored in the DACs output registers that provide the control voltages for each DC-DC converter.

All analog signals corresponding to the output voltage and load current values are fed consecutively through an analog multiplexer (MUX) to a 12-bit analog-to-digital converter (ADC) to be transferred (in serial mode) by the local control block to the controller. These signals are also sent to the individual channel comparators (CMPs), where they are compared with the voltage or current limit values received by the crate local bus. In case of overvoltage or overcurrent in any channel its comparator sends an alarm signal to the module control block, which immediately disables all three channels of the corresponding cluster, dropping the output voltages to zero.

The output high voltages of each module are fed by a multi-wire cable to a HV distributor from which 9 short cables transfer the supply voltages to the read-out boxes (roboxes) with PMTs. In order to control the integrity of all HV lines a daisy chained interlock circuit is added in the cables. At any interruption of the interlock circuits the module control block immediately disables all channels and activates the

module front panel LED (INTERLOCK). The interlock status of the modules is monitored by the controller.

Ten LEDs (1 in the HV distributor and 9 in the roboxes) indicate that at least one group of HV channels is on and high voltage is fed to the roboxes.

2.2. High voltage DC-DC converter

The electrical diagram of the DC-DC converter for −2000 V is shown in fig. 3. Due to the relatively low output current (0,8 mA) a linear voltage regulator (Q1) and a single transistor transverter (Q6, Tr, R1, R2, C2) are used. The negative output high

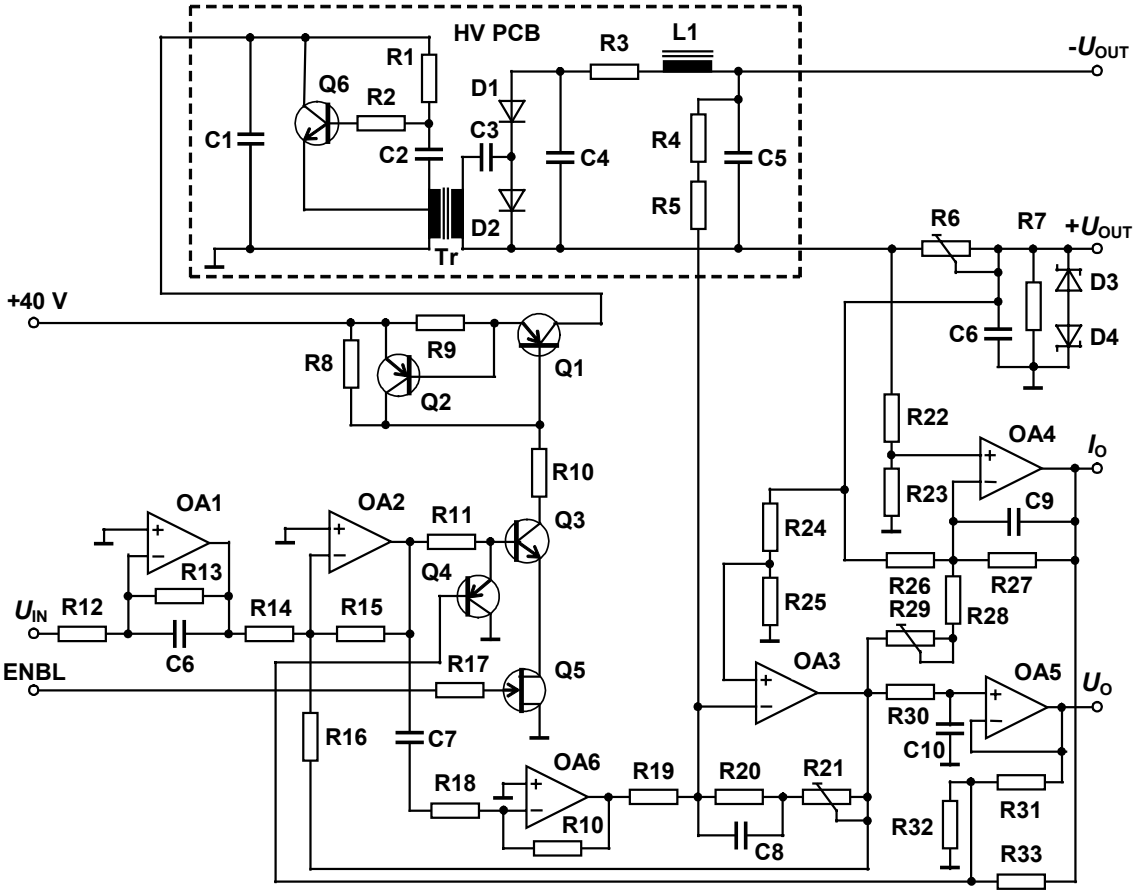

Fig. 3. Electrical diagram of the −2000 V DC-DC converter.

voltage (-U_{OUT}) is produced by means of a two stage Cockcroft-Walton circuit (D1, D2, C3, C4) and a RLC filter (R3, L1, C5). The output is floating (+U_{OUT} terminal) to facilitate single-point ground configuration. The voltage between this terminal and ground is limited by the Zener diodes D3, D4 (among about ±5 V).

The voltage regulator is supplied by +40 V. It's control voltage is fed to the input U_{IN}. The difference between amplified (in operational amplifier OA1) U_{IN} and the negative feedback voltage (received from the OA3 output) is amplified in OA2 and controls the linear regulator by the transistor Q3. The feedback signal in the OA3 output is used also for output voltage measuring – through the buffer OA5 it is fed to the U_O terminal. The voltage U_O can be adjusted by changing R21.

The output current is measured by means of the resistor R6 – the voltage over it is fed to the I_O terminal through OA4. In order to compensate the current through the negative feedback circuit (R4, R5) a supplementary current is fed by the resistors R28 and R29 (adjusted by R29) from the OA3 output to the OA4 inverting input.

There are two additional protection circuits in this DC-DC converter:

- the current limiter (Q2 and R9) limits the current through Q1, defining maximum dissipated power in the converter;
- in case of lack of output voltage or/and output current signals (through R31 or R33) the normally closed transistor Q4 goes to active state thus preventing Q3 and Q1 from saturation and limiting the current through the linear regulator.

A high pass negative feedback (C7, R18 and OA6) suppresses the self generation.

The other two DC-DC converters – for −800 and −400 V have almost the same electrical diagram.

2.3. Module local control block

The system controller uses a set of 12 instructions shown in Table 1. All bus operations are executed in two steps – first, an instruction code is transmitted and then the instruction is executed. Each instruction contains a four bit channel address (b0-b3) and a four bits operational co-de (b4-b7). So-me instructions can be executed simultaneously in a selected channel (cluster) in all modules (b4=0, ALL=1) or in all channels in all modules (b4=1, ALL=1). In order to execute the instruction the controller issues different number of clocks (see table 1).

Table 1. Instruction truth table.

Instruction code b7 b6 b5 b4 b3 b2 b1 b0	ALL	Clk's Nbr	Rd/ Wr	Data Flow	Description
1 1 0 x x x x x	0/1	1	Wr		Enable module and load ID
1 1 1 x x x x x	0/1	1	Wr		Disable module and load ID
0 1 1 0 c c c c	0/1	1	Wr		Clear Prot. Rgs – channel cccc
0 1 1 1 x x x x	0/1	1	Wr		Clear Prot. Rgs – all channels
0 1 0 0 c c c c	0/1	1	Wr		Set Prot. Rgs – channel cccc
0 1 0 1 x x x x	0/1	1	Wr		Set Prot. Rgs – all channels
0 0 0 1 x x x x	0/1	16	Wr	In	Load all DAC's shift registers
0 0 1 0 c c c c	0/1	1	Wr		Load DAC's output reg. – ch. cccc
0 0 1 1 x x x x	0/1	1	Wr		Load all DAC's output registers
1 0 x 0 c c c c	0	15	Rd	Out	ADC conversion – ch. cccc (voltage)
1 0 x 1 c c c c	0	15	Rd	Out	ADC convers. – ch. cccc (current)
1 0 x x x x x x	0	8	Rd	Out	Read module data register

cccc – channel address, x – don't care

The block diagram of the module control block is shown on fig. 4. Three lines are needed for serial data exchange between the controller and the module – bus clock (BCK), bus data read (BDR) and bus data write (BDW). The controller uses four address lines – MA0, MA1, MA2 and ALL to address the modules. When ALL=1, all modules are enabled for a write operation (ignoring all other address lines in this case). The module address is defined by three address lines (LA0, LA1 and LA2). The instruction transmission is enabled by IEn line. The interlock line (INTL) gives information about the high voltage cable net integrity. A bus reset line (BRES) is provided to initialize all modules and channels.

The main parts of the block are:

MAD – module address decoder; MS=1 when the module is selected (the bus address is equal to the local address or ALL=1);

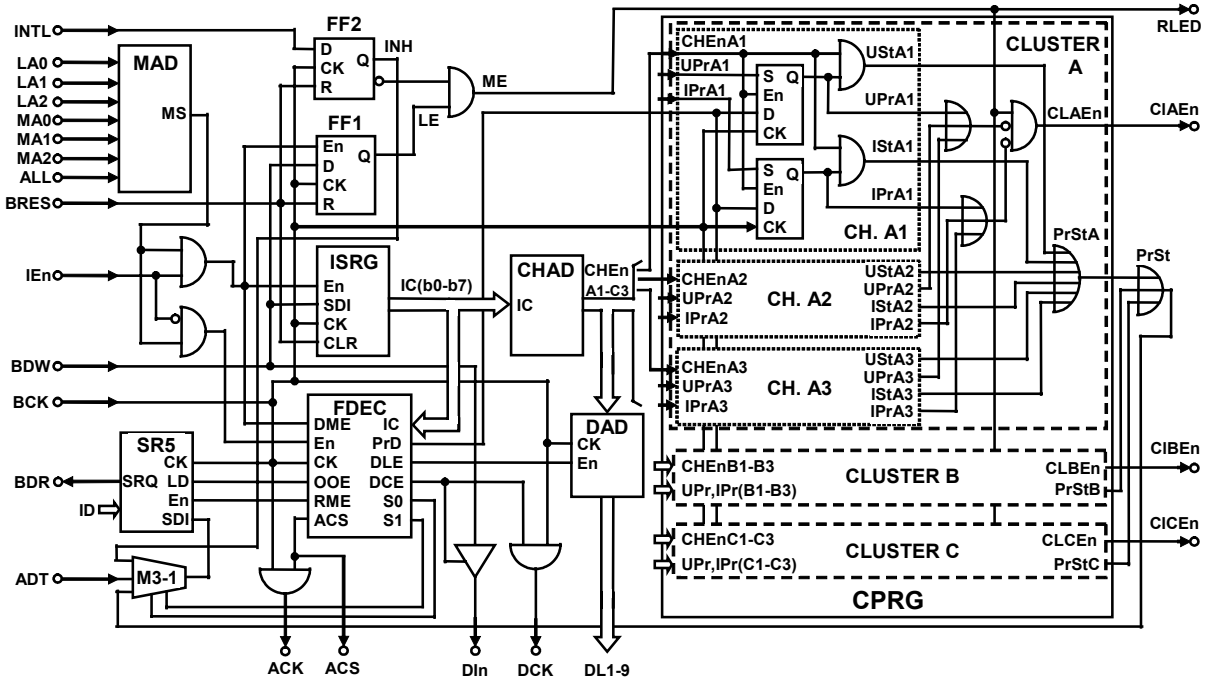

Fig. 4. Block diagram of the control module block.

ISRG – instruction register, in which the instruction code is stored; **ISRG** is loaded, when IEn=MS=1.

CHAD – channel address decoder – decodes individual channel addresses;

SR5 – five bits module data (shift) register;

FDEC – function decoder, in which the instruction stored in **ISRG** is decoded;

DAD – DAC address, which directs the data from BDW line to the DACs;

M3-1 – 3-to-1-multiplexer;

CPRG – channel protection register, in which the status of the protection circuits in all 9 channels is stored.

When the instruction "Enable (or Disable) module and load ID" is executed (DME=1) LE line is set/reset (Q1=1 or Q1=0) and the module predetermined 5–bits ID code is loaded in SR5 (**FDEC** output OOE=1). Thus the controller can recognize different type of modules in the crate. If LE=1 and INH=0 the module is enabled (ME=1). This signal enables all cluster AND gates in **CPRG** and if there is no overvoltage or overcurrent in the channels all cluster output voltages can be modified. In the same time ME signal activates all remote LEDs in the roboxes (output RLED) indicating possible high voltage at their connectors. INH is set when Interlock loop is interrupted (INTL=1). All channels are then disabled (ME=0).

Depending on the channel address, **CHAD** selects one (or all) channel. When a "Load DAC's shift register" operation has to be executed **FDEC** sets DCE=1 and a write operation in all nine serial DACs is performed (DCK and DIn line are used). If

a "Load DAC's output register" operation is decoded, DLE=1 and a write operation in addressed DAC(s) is executed (DL1-9 are used).

Fig. 5. HV power supply module.

The information about the voltage and current comparators status in all channels is stored in **CPRG** (UPrA1-C3) and IPrA1-C3 inputs). In case of an overvoltage or overcurrent in any channel the corresponding latch is triggered and the cluster is immediately switched off (ClAEn-ClCEn=0). The latches of each channel can be set or reset by the controller. If INH=1, all clusters are disabled (ME=0).

When **FDEC** outputs ACS=RME=1 the ADC conversion is enabled. Then the controller issues a series of 15 bus clocks. This series is applied to the module ADC clock input (output line ACK) and the serial data (d11-d0) from the ADC output (see fig. 2) are fed to the input ADT. The three leading bits of these data are meaningless and by means of the **FDEC** (outputs S0, S1) and the multiplexer **M3-1** two extra bits are incorporated – the status of INH and the status of the corresponding protection latch in **CPRG**. Thus the **SR5** block and through it the crate controller receive the following series of signals

0	INH	PROT	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0

A photograph of the HV power supply module is shown in fig. 5. The high voltage area is shielded by an aluminum plate.

3. EXPERIMENTAL RESULTS

Table 2. Basic module technical parameters.

PARAMETER	CHANNELS A1,B1,C1	CHANNELS A2,B2,C2	CHANNELS A3,B3,C3
Max. operating voltage, V	**2000**	**800**	**400**
Voltage resolution step, V	**0,5**	**0,2**	**0,1**
Ramp rate, V/s	**5 – 500**	**2 – 200**	**1 – 100**
Voltage ripple, mVp-p	**100**	**40**	**20**
Voltage monitoring inaccuracy, %	**< 0,1**	**< 0,1**	**< 0,1**
Long term instability, %	**< 0,1**	**< 0,1**	**< 0,1**
Max. output current, mA	**0,8**	**0,8**	**0,8**
Current monitoring inaccuracy, %	**< 1**	**< 1**	**< 1**
Special	**Floating output**	**Floating output**	**Floating output**

A prototype of the module was tested at CERN where it showed long-term stable work in real operating conditions. The measured values of its basic technical parameters are shown in

Table 2. The floating outputs facilitate a single-point ground configuration.

4. CONCLUSIONS

A high voltage module for power supplying of the photomultipliers in CMS Forward Hadron Calorimeter has been developed. It contains nine HV-channels, grouped in three clusters of three channels. The DC-DC converters used in the channels have a number of protections against their incorrect operations. The module is fully computer controlled using a module control block communicating with the crate controller by a custom interface. One prototype of the module as well as the program package was tested in CERN under real working conditions. This experience has shown the power supply system to be stable and reliable.

5. REFERENCES

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