ASYNCHRONOUS PARALLEL RESISTORLESS ADC

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A parallel analogue-to-digital converter architecture is investigated, which is based on CMOS inverters used as comparators. The comparator threshold voltage depends on the ratio of transistor areas. A stage with a so-called "dynamic hysteresis" is added to the design to increase the noise immunity. The advantages of such ADC are its fully digital structure, the lack of resistor ladder and the asynchronous mode of operation, which diminishes both area and power and makes it suitable for system-on-chip solutions. The static and dynamic characteristics of the device are examined and some recommendations for future investigation are outlined.

Keywords: parallel CMOS ADC, dynamic hysteresis

1. INTRODUCTION

The dynamic development of mixed-signal system-on-chip applications leads to a growing need of more sophisticated circuit designs in terms of speed, area and noise immunity. This is particularly important in ADC design, which is often the bottleneck in the design of SOC applications. The flash architectures constructed of latched comparators (Fig. 1a) are preferred for their speed and inherent monotonicity, but suffer from large area and power dissipation. In addition, the latched comparators cause substantial noises on the input signal (kickback noise [8]) and on the supply voltage lines. The present work focuses on the design of high noise immunity resistorless ADC with lower noise generation on the supply voltage lines. It is organized as follows: in Sect. I an overview of the problem is presented, Sect. II describes the method for V_{THI} determination; Sect. III gives the circuit analysis results.
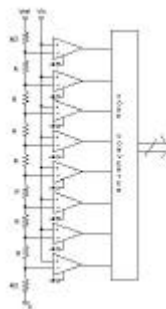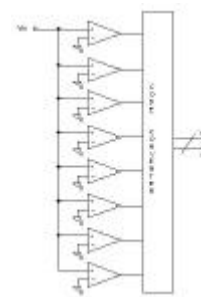

Fig. 1a. Traditional Flash ADC   Fig. 1b. Parallel resistorless ADC

In earlier works [1,4,6,7] a resistorless parallel ADC (Fig. 1b) was proposed that uses simple CMOS inverters instead of comparators. It operates asynchronously, i.e. the switching of the 2^n comparators is more or less uniformly distributed depending on the input signal. Thus the noises on the power supply lines are reduced and the

total power consumption compared to the pure flash ADC may be diminished from 2 to 5 times depending on the input signal shape. Another advantage of the ADC is its smaller size compared to the traditional flash architectures.

In [2] a similar architecture is proposed. It consists of two cascaded threshold inverter comparators (TIC) and a gain boosting stage. The comparator threshold voltages V_{THI} are obtained by simulation. In standard 0.25μ CMOS technology the authors obtain an operation speed of 1 GSPS. In [3] command logic is added to the design to turn off part of the comparators and change the ADC resolution, thus exponentially diminishing the power consumption.

The present paper applies the method for standard 0.18μ and 0.07μ CMOS technology. An investigation of the static and dynamic behaviour of the ADC is performed to explore its maximal resolution and frequency of operation without missing code. The boosting stage used in [2] to increase the comparator gain was replaced by a Schmitt trigger with time controllable noise immunity developed by the authors [6,7].

2. THRESHOLD VOLTAGE DETERMINATION

The threshold voltage V_{THI} of the inverter depends on the transistor area ratio of the N-channel and P-channel MOS transistors. The analytical solution for V_{THI} given in [5] neglects the short channel effects and is not applicable small die size technologies. The dependence of the threshold voltage on transistor area ratio was obtained by simulation (Fig. 2), the non-shaded part corresponding to the voltage full-scale range. The comparator parameter values were as follows: $V_{DD} = 2.5V$, $k = 0.45 \div 20$, $W_N/L_N = \text{const}$ for 0.18μ CMOS, and $V_{DD} = 1.5V$, $k = 0.2 \div 20$, $W_N/L_N = \text{const}$ for 0.07μ CMOS. A *PSpice* macro was used to construct the step function, from which the values of transistor area ratio k for a chosen level of quantization were generated automatically. This procedure is easily adaptable to different transistor models, input voltage full-scale range and ADC resolution.
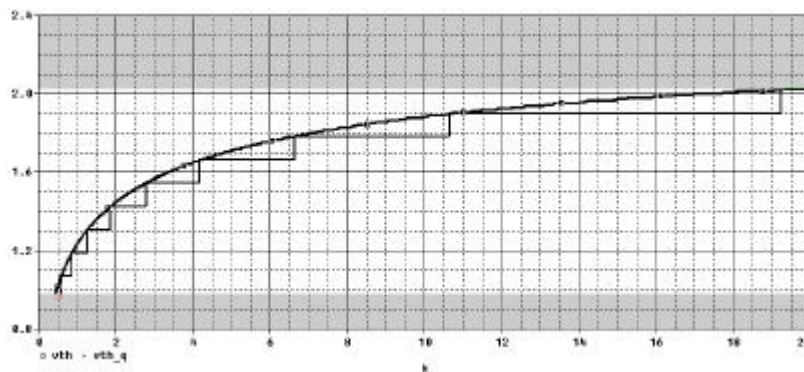

Fig. 2. Inverter threshold voltage V_{THI} as a function of transistor area ratio k

3. ADC INVESTIGATION

The method of area size determination was applied for a level49 BSIM3v0.0 0.18μ CMOS technology with minimum square size of 0.44μ and 0.07μ CMOS technology with minimum square size of 0.2μ. As an example a 3-bit ADC was simulated and eight values of k were determined.

It can be seen that comparator areas do not follow the uniform resistor ladder voltages by a binary exponential low, as it could be expected (Table 1). The comparator size depends only on the input voltage full-scale range. For instance, for $V_{FSR} = 950$ mV, the top-most level comparator transistor area ratio k is kmax = 9.882, regardless of the chosen resolution which leads to a substantial ADC area saving.

Table 1. Transistor area ratio

0.18μ CMOS, V_{FSR} = 0.95V			0.07μ CMOS, V_{FSR} = 0.7V		
V_{THI}, V	k	P?/N?	V_{THI}, V	k	P?/N?
1.06875	0.644	0.18 / 0.28	0.6125	0.377	0.07 / 0.19
1.1875	0.911	0.18 / 0.19	0.7	0.577	0.07 / 0.12
1.30625	1.311	0.24 / 0.18	0.7875	0.866	0.07 / 0.08
1.425	1.889	0.34 / 0.18	0.875	1.333	0.09 / 0.07
1.54375	2.711	0.49 / 0.18	0.9625	2.088	0.15 / 0.07
1.6625	4.111	0.74 / 0.18	1.05	3.377	0.24 / 0.07
1.78125	6.155	1.11 / 0.18	1.1375	5.577	0.39 / 0.07
1.9	9.822	1.77 / 0.18	1.225	9.666	0.68 / 0.07

3.1 Inverter transfer characteristics

The values of the threshold voltages V_{THI} were recorded at the point of the transfer characteristic where the input voltage of the inverter equals its output voltage. A grid of equally spaced characteristics was obtained. Afterwards, as in [2], a stage of two cascaded inverters was used to increase the gain and to sharpen the transfer characteristic. For the boosting inverter a transistor area ratio 8/4 was chosen so that the switching occurs at half of the input voltage full scale range and the rising and falling edge delays are approximately equal.

3.2 Inverter dynamic behaviour

The time-domain analysis shows that the proposed ADC may operate at speeds up to approximately 1GHz. For an input signal with frequencies higher than 0.1GHz however, some shifting arises in inverter switching due to its finite gain. That is, the switching of the comparators for the rising and the falling edge occurs at different threshold voltages which may lead to subsequent decoding errors.

The inverter delays for each bit of the ADC have been investigated. The rising edge delay is constant, because of the constant size of the NMOS transistor, while the falling edge delay depends strongly on the increasing size of the PMOS transistor and is dominant for the overall dynamic behaviour of the inverter for larger values of k. The delays for 0.18μ CMOS technology are approximately 3 times higher than the ones for 0.07μ CMOS.

3.3 Schmitt trigger with dynamic hysteresis

The second inverter of [2] was replaced by a boosting stage consisting of a Schmitt trigger with time-controllable noise immunity and a single threshold [4,6,7]. It consists of a CMOS Schmitt trigger and a delayed negative feedback loop (Fig. 3).

The trigger operates as follows: after the switching of the input inverter through the positive feedback (PF) the output inverter pulls up or down the voltage of the intermediate point "1" and thus the output is insensitive to eventual noises on the input signal. The period of insensibility depends on the odd number of inverters

connected to the trigger output. Afterwards the delayed negative feedback (DNF) turns off the positive feedback and the output becomes sensitive to changes on the input signal again. This mode of operation is called by the authors "dynamic hysteresis", because the trigger switches at the same threshold voltage for rising and falling signal, and the hysteresis occurs in time, rather than on the input voltage.
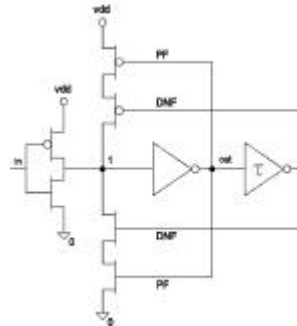

Fig. 3 Dynamic hysteresis trigger circuit

To obtain the transfer characteristics of the Schmitt trigger, the delayed negative feedback must be switched off, i.e. the N-channel and P-channel transistors that it commands are tied to the power supply voltage and to the ground voltage respectively. The resulting transfer characteristic shows that the gain of the Schmitt trigger circuit is significantly greater than that of the inverter booster.
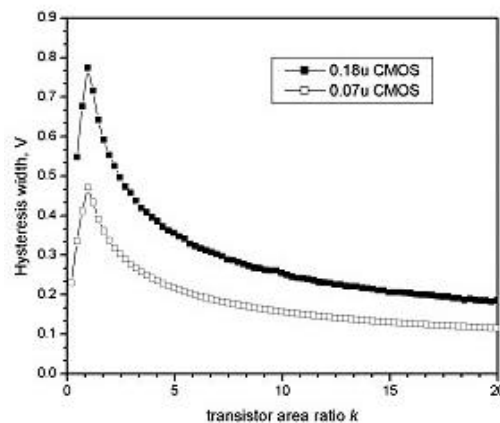

Fig. 4. Maximal noise magnitude that can be suppressed as a function of k

The same settings are used to obtain the width of the hysteresis of the trigger in dependence of transistor area ratio k for the two investigated technologies (Fig. 4).

The value of the hysteresis for each bit of the ADC corresponds to the maximal magnitude of the noise on the input signal that can be suppressed during the switching of the comparator (Fig. 5). Any noise with larger magnitude leads to an erroneous spike in comparator output which may produce an error during the subsequent conversion of the thermometer code to code 1-of-n (Fig. 6).
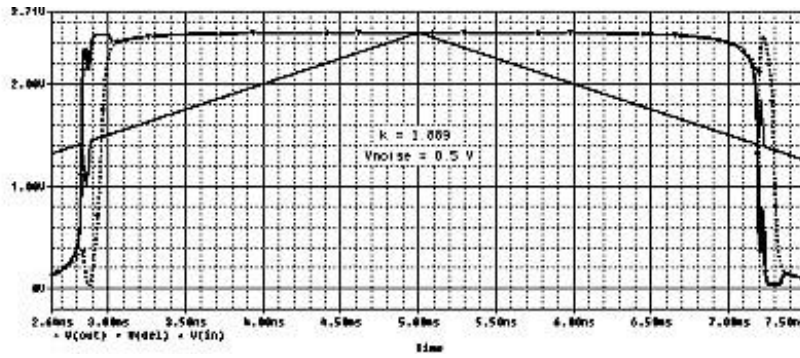
Fig. 5. Successful noise suppression (solid) and erroneous output of the inverter circuit (dashed)

Previous experiments prove that with appropriate transistor sizing of the Schmitt trigger the noise immunity for the rising and the falling edge of the input signal may be equalised [7].
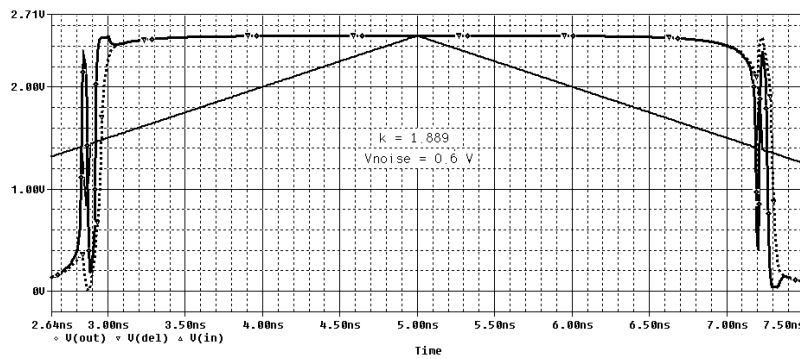

Fig. 6. Noise with larger magnitude leads to erroneous switching of Schmitt trigger (solid) and inverter (dashed)

3.4 Dynamic behaviour

The investigation of the comparator delays for each bit of the ADC is given in Fig. 7 for 0.18µ CMOS technology. It can be seen that the circuit with two cascaded inverters shows a larger delay than the one with a Schmitt trigger. This holds as well for the output in 1-of-n code of the inverter booster stage which is distorted and for higher frequencies may cause erroneous further decoding due to magnitude failures or to variation of the exact moment of the switching. On the other hand for lower frequencies it may be preferred for its simpler design and less power consumption in comparison with the dynamic hysteresis Schmitt trigger.
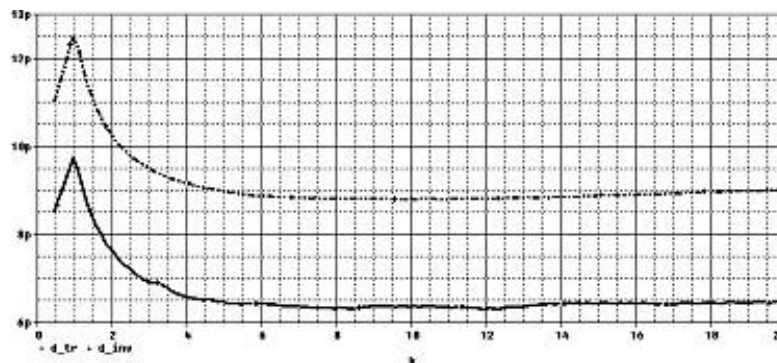

Fig. 7. Comparator delays as a function of k for an inverter booster (dashed) and a Schmitt trigger booster (solid)

4. CONCLUSION

Some aspects of the design of a high-speed parallel resistorless ADC based on CMOS inverters were investigated. The operation of the ADC is verified for 0.18μ and 0.07μ CMOS technology. Its static and dynamic behaviour was explored. The implemented example proves the benefits of the design which make it suitable for SOC applications, with smaller size and power consumption.

The results of the ADC investigation show that scaling of the design may be a challenge. Although its dynamic behaviour is weakly affected, its full scale range voltage and its noise immunity decrease.

Nevertheless some aspects of the design of the proposed ADC have to be further investigated:

- The delays of the different comparator stages are different and may cause missing codes for higher frequencies.
- The dependence of the shifting in comparator switching on input signal rising and falling edge has to be studied. Together with the effect of the different delays of the comparator stages, this issue may turn out to be dominant for the overall ADC dynamic behaviour.
- The influence of the technological process variation as well as the truncation or rounding of transistor area ratio k needs more comprehensive investigation especially for smaller die sizes.
- A drawback of the comparator is that the input is not differential. This can be mitigated by a differential amplifier at the ADC input. The same amplifier could be used to shift the analogue input voltage to the ADC voltage range.
- An optimal solution for subsequent code conversion as well as the synchronization of the ADC output has to be elaborated.

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