DESIGN OF MIXED SIGNAL CIRCUITS AND SYSTEMS FOR WIRELESS APPLICATIONS

Vladimir LANTSOV

Computer Engineering Department, Vladimir State University, Gorky Street, 87, 600026, VLADIMIR, Russia, phone: +7 0922 279808, e-mail: lantsov@ieee.org

Keywords: mixed signal circuits and systems, design, wireless applications

The wireless communication systems design plays the important roles in the field of microelectronics and system-on-chip methodologies. Traditional digital, mixed signal and analog low-frequency designers have enjoyed an integrated front-to-back IC design system. On the other hand, radio frequency or microwave designers with a discrete design background have used board-level computer-aided design (CAD) tools. The objective of this paper is to present some results of research work in the field of RF analog and mixed signal wireless communication systems design. We also discuss the challenges facing microelectronics in modern wireless communications systems. Analog and mixed signal design methodologies and simulation problems as well as modern CAD tools for mixed signal circuits and systems are discussed.

1. THE INTRODUCTION

The expansion of the market for portable wireless communication devices has given a tremendous push to the development of a new generation of low-power radio frequency (RF) and mixed signal integrated circuits products. In this fast-growing environment where time-to-market constraints force tight schedules, having a good design methodology, modern computer-aided design (CAD) tools and a well-integrated design system are key factors to success.

In recent years, RF design has undergone a paradigm shift as more and more RF functions have been integrated on a single chip and the number of discrete components has decreased. This trend is more evident in the low-power segment of wireless communications market, which includes handsets for cordless and cellular phones, pagers, and now Bluetooth standard. Even though RF designs contain fewer devices compared to digital chips, they are inherently more challenging, as very little automation is available for the design process. Moreover, RF devices are typically pushed to their performance limits; thus, all the nonlinearities and second-order effects need to be taken into account.

Historically, IC and RF designers have used different design methodologies, tools, and practices. Traditional analog designers have enjoyed an integrated front-to-back IC design system. On the other hand, RF designers with a discrete design background have used board-level computer-aided design (CAD) tools. With IC applications approaching several gigahertz and the appeal of monolithic design because of the growing device speed, silicon is bridging the gap between traditional low-frequency analog design and discrete RF design, bringing the two worlds together in order to provide better and cheaper solutions for consumers.

The objective of this paper is to present some results of research work in the field of RF analog and mixed signal wireless communication systems design. We also discuss the challenges facing microelectronics in modern wireless communications systems.

2. MICROELECTRONICS IN MOBILE COMMUNICATIONS

In some European countries today the number of cellular phone users exceeds the number of installed telephone lines. Microelectronics made mobile terminals successful by offering low-cost solutions and continual improvements in features and in autonomy—that is, talk time and standby time (reflected mainly in battery life). For example, a lower power requirement (reduced from 5 V to 2 V) has increased autonomy, and the move to submicron-CMOS processes (from 1 micron to the current 0.09 micron) has reduced power consumption. For example, a GSM terminal has two sections, each specific in terms of its technology requirements.

Fig. 1 shows the inside of a modern cellular (GSM) terminal. As can be seen from the "inside" picture (Fig. 1), the front-end part contributes significantly to the size of the total handset.

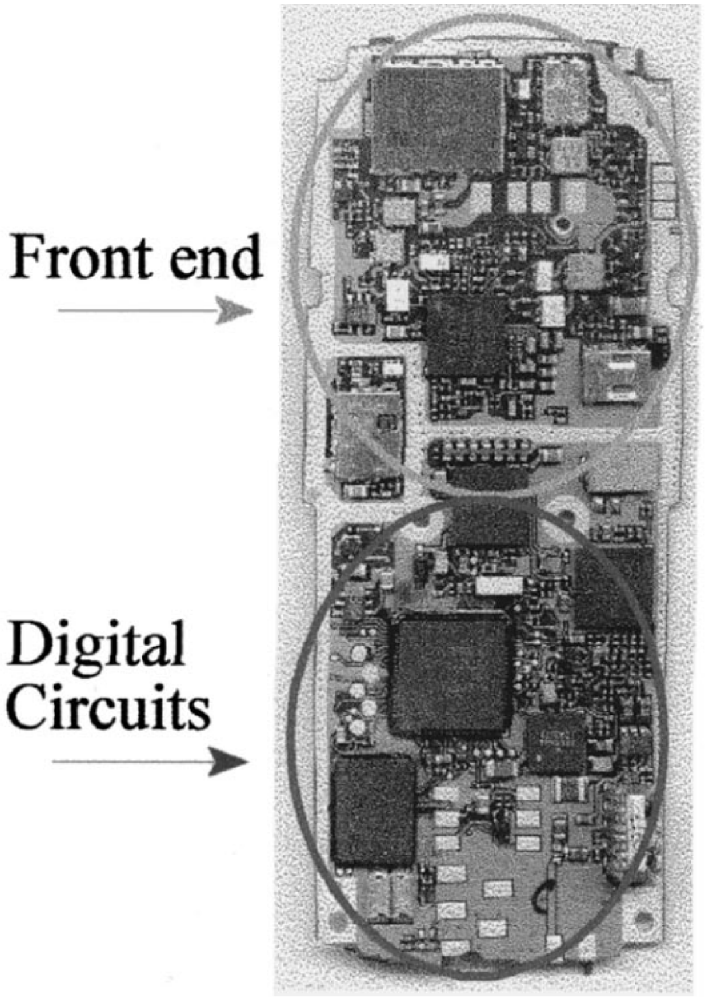

Fig.1. Inside of GSM handset.

The radio section is mainly analog; its implementation requires many passive elements whose integration on silicon is often difficult. Radio accounts for most of the terminal's power consumption (60% to 70% in communications mode). The radio section consists of a very limited number of active devices, often in the order of hundreds or thousands. The silicon area of the front end decreases with improvements in IC technology, and currently measures just a few square millimeters. Also, the desired functionality and therefore the number of active devices decreases with advanced transceiver architectures such as single-conversion receivers, and further digitization of the radio. Compared to the millions of transistors in the digital parts of a handset and the millions of bytes in the software, it might be assumed that the design of an RF front end is a trivial job, with little relevance for the overall handset. From such a viewpoint, it would be hard to justify any research in this area. Fortunately for RF researchers, the RF design problem is highly relevant.

Also, the total power consumption is dominated by the radio rather than the digital circuits, which has an additional impact on size and cost through the battery size: both in transmit and in receive mode, more than 60% of the total power is consumed by the radio in a typical cellular handset. Therefore, the RF front end has a major impact on achieving the design goals of a small and cheap phone.

The digital section, implemented with a few CMOS components, processes digital data. It comprises a microprocessor (RISC machine) and a digital signal processor (DSP). These components have progressed dramatically in terms of cost and performance with their move to submicron-CMOS processes.

2.1 Radio Section

Radio architecture has evolved impressively over the last decade. The well-known heterodyne receiver, with its bulky passive filter and multiple oscillators, has been progressively replaced by simpler and more integrated architectures based on direct conversion or low intermediate frequency (IF). When radio was first employed for cellular networks, the low-noise amplifier used discrete devices. The power amplifier remained an impressive hybrid module. Up and down converters were already integrated as a single bipolar chip. Then the low-frequency analog functions were typically implemented in two specific chips plus a separate synthesizer. Compared with previous radio solutions, this approach drastically reduced the number of devices and passive elements. The next natural evolution was the merging of low-frequency functions into a single 5-V CMOS device. Integrating filters, amplifiers, the AD converter, and a limited number of digital blocks for control purposes wasn't difficult. More ambitious was the integration of the phase-locked loop. Very tough spectral purity requirements (especially with direct conversion) appeared difficult to meet in a complex mixed mode circuit.

Most IC design centers are working on a one-chip radio, using one of two approaches: merging the analog baseband chip with either the RF circuit or the digital CMOS chip. The first solution takes full advantage of dedicated BiCMOS technologies. Integrating the low-frequency analog function in a digital chip and

using standard digital CMOS results in the best price. In parallel with the reduction in chip count and equivalent silicon area, a significant effort is directed at power consumption.

2.2 Digital Section

A first-generation digital section contained three application-specific integrated circuits (ASICs) and three standard ICs. Because of ever-shrinking silicon technology and efforts to reduce cost and power consumption, current implementations use a single CMOS ASIC plus two standard ICs. The declining number of chips led to the use of CMOS technologies, which shrunk from 1 micron to the present 0.09 micron. Today the two standard components are an SRAM (static random-access memory) and a flash memory. The digital base-band chip performs speech coding and decoding (full rate, half rate, and enhanced full rate), channel coding and decoding, synchronization, demodulation, and ciphering. Its other functions include voice activity detection and discontinuous transmission. The digital base-band chip's high level of integration reduces board area and component count. Supply voltage ranges from 1 V to 2.7 V, depending on the operational modes.

2.3 3GPP Terminal Challenges

An each of the two main sections (RF and digital) of a 3GPP (Third-Generation Partnership Project) terminal faces specific challenges related to cost, volume, and power consumption.

RF section. Multimode and multiband services affect mainly the radio section. With such a front end, using today's technologies for switches and filters, the degradation, compared with that of a mono-band terminal (say, a 900-MHz GSM front end), can reach 2 dB of noise for the receiving section and an equivalent value after the power amplifier. Moreover, such a solution results in a much larger board surface. To limit performance degradation, control costs, and restrict board surface, researchers are studying: the use of embedded filters and switches in the silicon process; trackable filters to limit the number of filters and switches; technologies with reduced noise to reduce filtering constraints—for example, GaAs and SiGe are good candidates, and the BiCMOS SiGe process offers a higher level of integration for RF functions; wideband architectures with, for example, direct conversion (zero- or low-IF solutions) that provide a high level of integration by moving the major part of the analog functions into the low-frequency domain, where programmable filters are much easier to implement; and active control on power amplifiers to improve linearity and efficiency.

Digital section. The multimode and multiband aspect of 3GPP terminals has much less impact than the complexity of the digital functions. The high bit rate of 3GPP systems (now 3.84 megacycles per second) is the dimensioning factor of the complexity. Today a GSM terminal's digital functions are implemented with two memories and a digital base-band chip. Base-band chip complexity depends mainly on the processing power required by a 3GPP system, which affects mainly the DSP and the buffer size. With the use of the latest CMOS technologies (0.09 micron),

which provide very high levels of density, the digital chip's size will be quite acceptable in terms of cost. The 3G system challenges affect mainly the radio section.

3. WIRELESS DESIGN METHODOLOGIES

The design of RF and mixed signal ICs and full wireless communication systems are strongly influenced by several factors. At the wireless system design level, the choice of frequency band, modulation scheme, and duty cycle has a major bearing on power consumption. For a given system design, the radio architecture, algorithms of demodulators, choice of IC implementations, and good circuit design all play a role. There are different Tolls and design methodologies for wireless systems design. But the main problem of most of modern CAD tools is the difficulties of transfer of specifications from system levels to circuit levels and implementations. One of such modern methodologies is based on software-defined radio technique (SDR). With this technique, only one infra-structure hardware system would need to be developed. The difference in frequency bands and technology standards would be implemented by loading different software into the system. This approach becomes possible because of the rapid progress in semiconductor and digital technologies. More specifically:

• The advances in analog-to-digital (A/D) and D/A conversions have made it possible to directly convert signals closer to the antenna at high speed with adequate dynamic range. This reduces the radio components needed and greatly facilitates digital implementation.

• With the signals converted to digital in the very early stages of the system at high speed, a wideband radio approach can be adopted that provides inherent flexibility to support different standards which operate with different frequency bandwidths.

• The rapid growth in the use of general-purpose digital signal processing (DSP) and field programmable gate array (FPGA) chips makes it commercially viable to manufacture general-purpose programmable devices at low cost. Furthermore, the speed of these devices using software is now adequate, and its performance can be comparable to that of a hardware implementation.

In addition to the advantage of being able to support different standards with a unified platform and hardware, SDR also has the following possible benefits: many commercial digital architecture and software protocol stacks are already available and can be used to further reduce the cost and the time to market; it will be much easier to introduce new services and features with software upgrades; the implemented system can easily be tailored to specific customer needs for both mass and niche markets; it provides flexibility to optimize the system performance over time and reduces new system deployment risks.

4. CAD TOOLS, RF AND MIXED SIGNAL METHODS OF ANALYSES

A very known SPICE-like programs provides several different types of analyses that have proven themselves essential to designers of baseband circuits. These same analyses are also needed by RF and mixed signal designers. The basic SPICE analyses include dc, ac, noise, and transient. RF versions of each have been

developed in recent years based on three different foundations: harmonic balance, shooting and Volterra-series methods.

Currently, the three dominant commercial RF simulators are ADS, a harmonic balance-based simulator from Agilent Technologies, SpectreRF, a shooting method-based simulator from Cadence, and Eldo RF from Mentor Graphics. ADS is generally preferred for board-level design, whereas SpectreRF and Eldo RF are the simulators of choice for integrated circuits. In additional, Microwave Office from AWR is Volterra-series based simulator.

A few years ago, there were clear distinctions between the capabilities of harmonic balance, shooting and Volterra-series method-based simulators. Over the years, the differences became less stark as harmonic balance simulators adopted Krylov-subspace methods [3] and shooting methods gained the ability to handle frequency-domain models. However, differences remain. Harmonic balance and Volterra-series provide better accuracy and efficiency when the circuit is near linear and the voltage and current waveforms are near sinusoidal, whereas shooting methods provide better accuracy, efficiency, and convergence properties when the circuits are strongly nonlinear.

5. CONCLUSION

In this paper we have analyzed the problems for RF and mixed signal for wireless communications systems design. The author would like to thank the REASON project for support this work.

6. REFERENCES

[1] M. Addra, D. Castel, J. Dulongpont, P. Genest, "Microelectronics in mobile communications: a key enabler,"IEEE Micro", pp.62-70, Sep-Oct. 1999.

[2] R. Telichevesky, K. Kundert, J. White, "Efficient steady-state analysis based on matrix-free Krylov-subspace methods,"Proc. IEEE/ACM DAC Conf.", June 1995.

[3] V. Lantsov, A. Merkutov, M. Morozov, S. Mosin, "Research and Training of RF Analog and Wireless Systems Design of Vladimir University, and Actions for Reason Project," Proc. of 9th International Conference - MIXDES'02. Mixed Design of Integrated Circuits and Systems. – Wroclaw, Poland, June 20 – 22", 2002, pp. 125-128.