ACTIVE GATE DRIVERS FOR MOSFETS WITH CIRCUIT FOR dv/dt CONTROL

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At this article is presented one scheme realization and exploring at active gate control of MOSFET, by the method at directly measuring at Drain voltage and of negative feedback by du/dt. Described is the applications method and is made analysis at transient processes at the scheme for control. The graphical aspect of transient processes at control circuit and at power circuit of MOSFET are given, adequately at status turn - on and turn - off. The principle of active gate control is improved losses and EMI emission in power converters.

1. INTRODUCTION

Active *di/dt* and *dv/dt* control is achieved in modern research by feedback control of the gate current based on the device current or voltage slopes. Sensing current or voltage slopes is carried out by: direct sensing [shunt resistor or Kelvin emitter]; using information resulted from Miller effect sensing [does not need galvanical separation]. The goal of this active control can be: Reduction of the EMI emission and Reduction of snubbed circuits [1,2,3]. Turn-on waveforms are adjusted through a gate control voltage waveform. An intermediate voltage level is introduced in order to decrease the gate current level on the first slope of turn-on. The voltage level and the length of the time interval with this voltage level can be adjusted [4]. The drain current can be limited beyond a maximum rate of rise by selecting appropriate *Vs*. The MOSFET would behave as an inductor with variable inductance. Measured radiated EMI is proving the advantage of reducing the *di/dt* slope [5]. After establishing the gate control voltages and gate resistors, the design of the gate driver continues with defining the power level of the control signal. The necessary power is a function of operating frequency, bias control voltages and total gate charge. The total gate charge is published in MOSFET datasheets, depending on gate control voltage. The average current can be calculated by: $iS = Q \bullet freq$. The total power can be estimated as $P = iS \bullet (VG+ - VG-)$. Usually this power is small. The tougher criteria for design is ensuring the peak gate current that can be roughly estimated as: $IG_{(Peak)} = (VG+ - VG-)/RG$ when a single gate resistor is used. Total losses can be calculated by adding up the switching and conduction losses while taking account of the inverter topology, the modulation function for each device and the operation mode or load power factor. In this article is described advanced method of active gate control. This method is based on direct sensing. This method is derived from series connected MOSFETS. Main constraints against an easy implementation:

– Fast event time scale that does not allow too much delays within the circuit;
– Feedback dependence on MOSFET parameters.

2. THE NEW DRIVING CIRCUIT FOR DU/DT CONTROL

In the researched scheme (Fig.1) the function at sensor for voltage is performing from serial connected resistors divider R13, R12. This drive circuit is designed for control of power MOSFET – VT4. The passive differentiation circuit is realized, including the elements R11, C2 and R10. Derivative value of drain voltage - Ud is receiving over resistor R10.

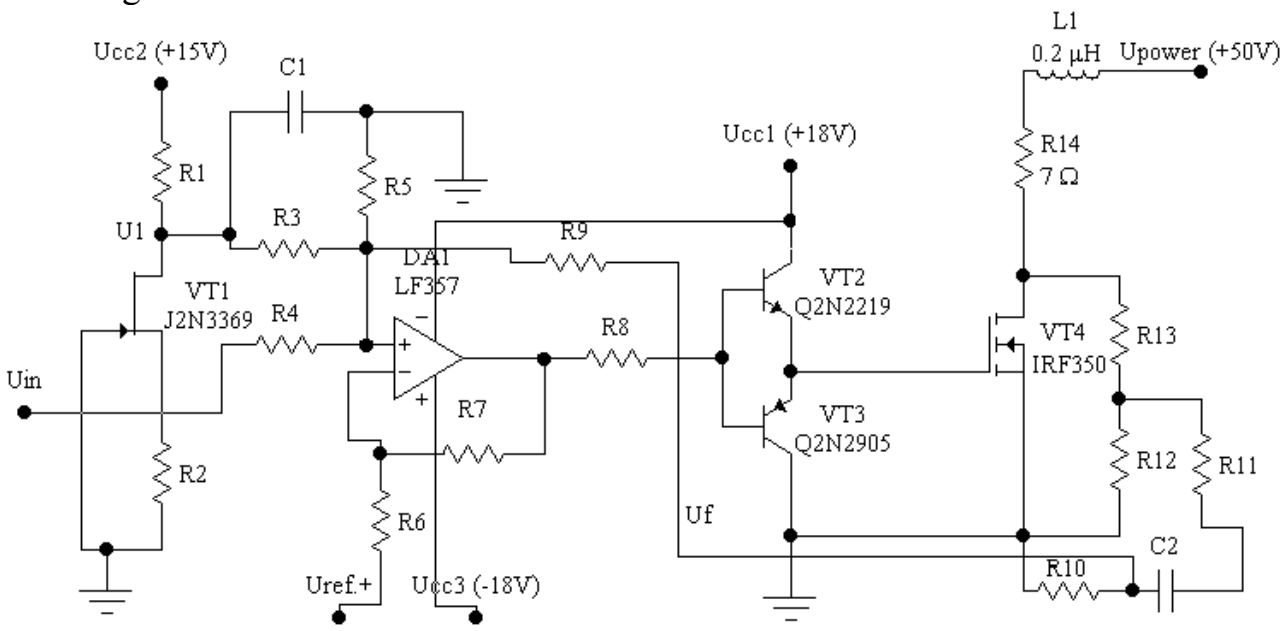

Fig.1

The receiving signal is amplified from single amplifier realized with DA1. The output signal from last amplifier represent signal of feedback connection by derivative to drain voltage – U_f. The input resistance of derivative circuit is capacitive, there by stability is low. For improving of stability and good SNR, the resistor R11 is serial connected with C2, and derivative group includes resistor R10 and C2. The transmission function at that case for derivative circuit would be equal at:

(1) $$U_d = \frac{p\tau_1}{1 + p\tau_2} \cdot \frac{U_{DS} R_{12}}{R_{13} + R_{12}}$$

Where: $\tau_1 = R_{10} C_2$

$\tau_2 = R_{11}.C_2$ and $R_{10} > R_{11}$

U_{DS} is drain to source voltage of VT4.

The value of resistors R8 is choused from the condition for suppressed hesitated process, conditioned by passed frequency band for stage amplifier of DA1.

The control voltage for push-pull emitter repeater (transistors VT2 and VT3) is output voltage of DA1. This voltage can be calculated by the relationship

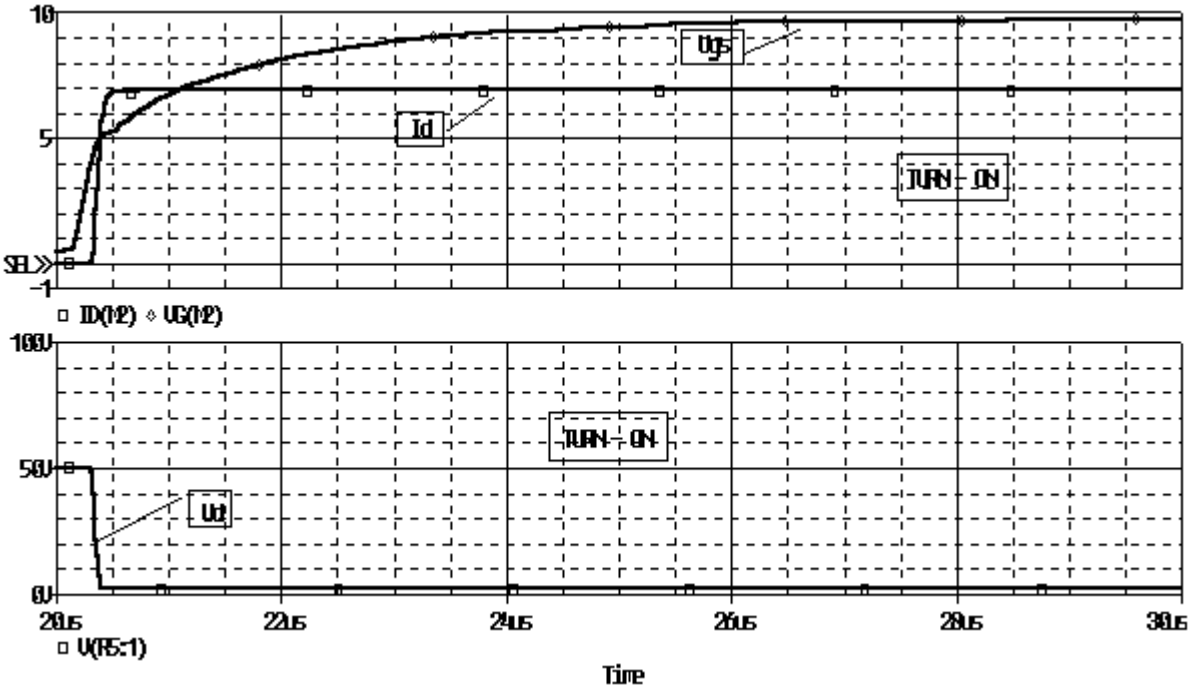

Fig.2

(2) $$U_{DA} = \frac{R_5}{R_4}.U_{in} + \frac{R_5}{R_3}.U_1 + \frac{R_5}{R_9}.U_d - \frac{R_7}{R_6}U_{ref.}$$

Where: U_{in} *are* input control rectangular pulses.
U_1 *is* constant value from drain of VT1
U_{ref} is a refugee voltage, which can be tune up.

After the turn-on delay period the drain current rises as the drain voltage falls (Fig.2).

(3) $$dU_{DS}/dt < 0 \ \ and \ \ U_d < 0$$

The gate-to-source voltage U_{GS} follows equation

(4) $$U_{GS} = (U_{DR} - U_T).(1 - e^{-t/T_G})$$

Where: U_T is gate threshold voltage of VT4;
$T_G = R_{in}.C_{GS}$.

Expressions for the gate voltage after turn-off delay period is follow (fig.3):

(5) $$U_{DA} = \frac{R_5}{R_3}.U_1 + \frac{R_5}{R_9}.U_d - \frac{R_7}{R_6}U_{ref.}$$

In this case

(6) $$dU_{DS}/dt > 0 \ \ and \ \ U_d > 0$$

Design is based on:
– Reduced delay time at both turn-on and turn-off
– Reduced turn-on di/dt and the associated reverse recovery effects

– Controlled overvoltage at turn-off

Reduced total switching losses at both turn-on and turn-off

Three intervals are defined for both turn-on and turn-off.

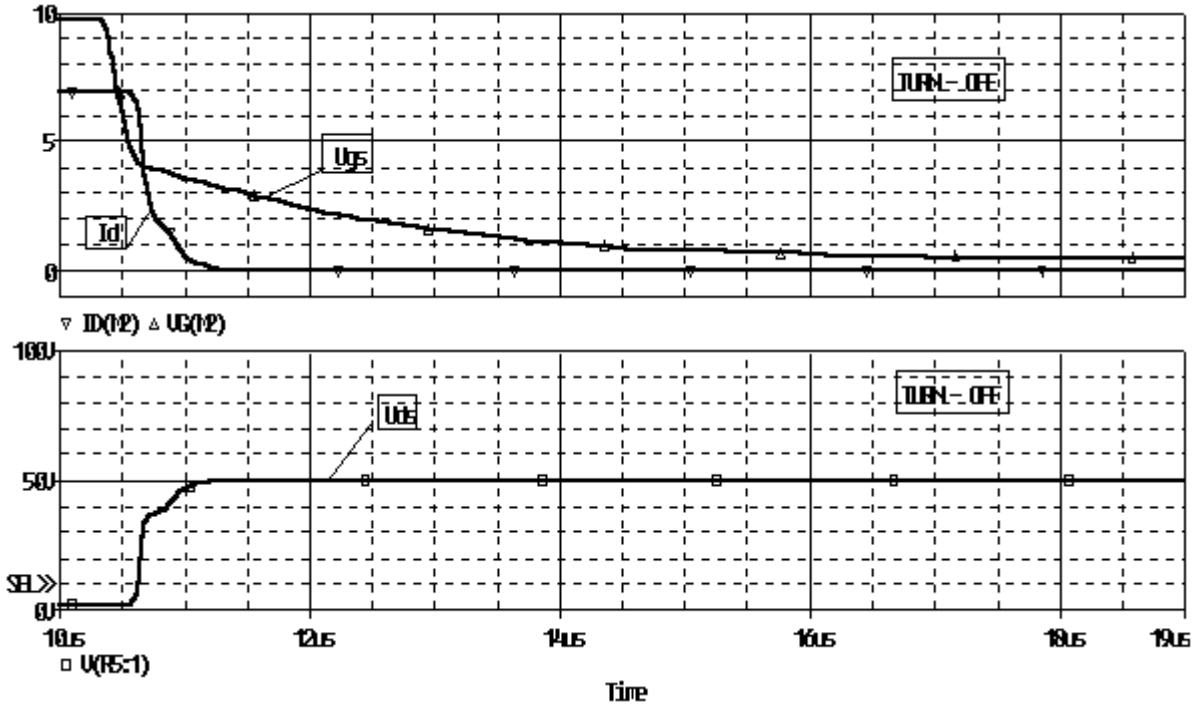

Fig.3

3. TURN-ON

First interval: Follows the turn-on command. MOSFET should be charged fast by a large gate current in order to minimize the delay time (Fig.2 and 4).

Second interval: Starts when the gate voltage reaches the MOSFETSs threshold level. The current injected into the gate is reduced to minimize the effects of the reverse recovery current, the associated overvoltage and the generated EMI. This interval ends when the drain current reaches the load current plus the peak reverse recovery current. **Third interval**: Gate is again rapidly charged to reduce the tail voltage thus reducing the power losses at turn-on.

3.TURN-OFF

First interval: Gate-source capacitor should be discharged fast until the rising instant of the drain voltage. Turn-off delay and the power switching loss are reduced (Fig.3 and 5). This large gate current pushes the gate voltage below the threshold level producing a large dv/dt with low power loss. Second interval: Starts when the drain voltage starts to rise by reducing the gate current. The rise of the drain voltage produces a displacement current through the gate-drain capacitance. The gate voltage tends to go up. This reduces turn-off di/dt and accordingly the turn-off over voltage. Third interval: starts at the end of the falling of the drain current. During this interval,

the gate voltage should rapidly reach its final negative level. A low gate resistance achieves this. The switching time is reduced as well as the noise immunity during the off state.

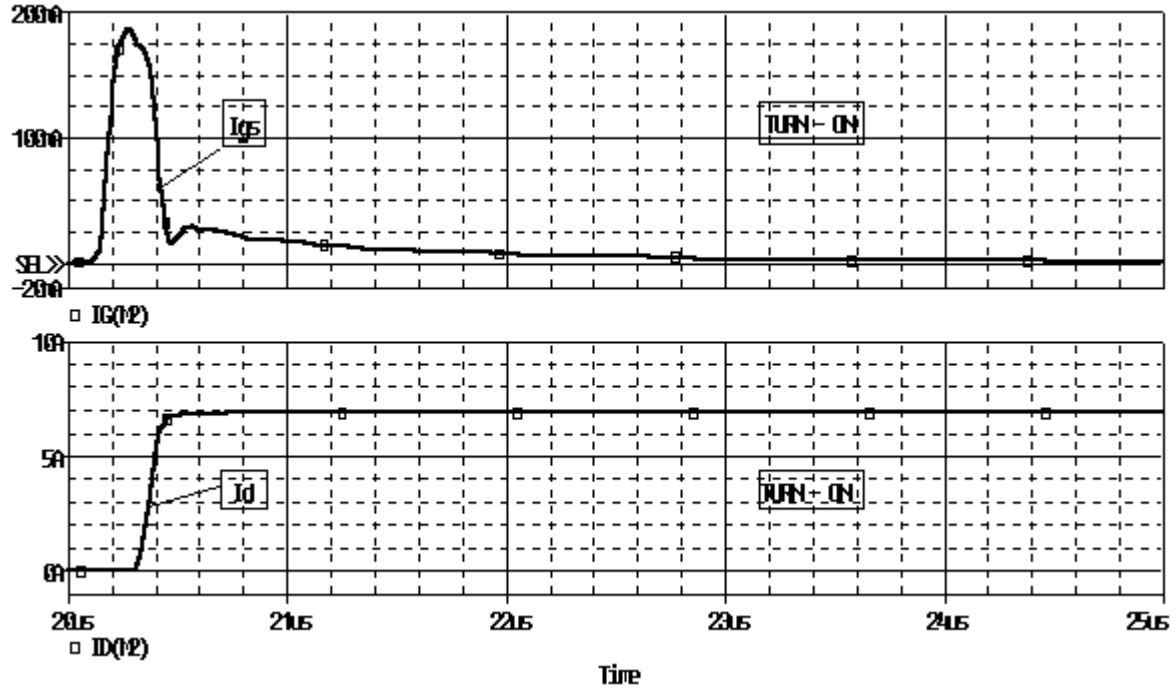

Fig.4

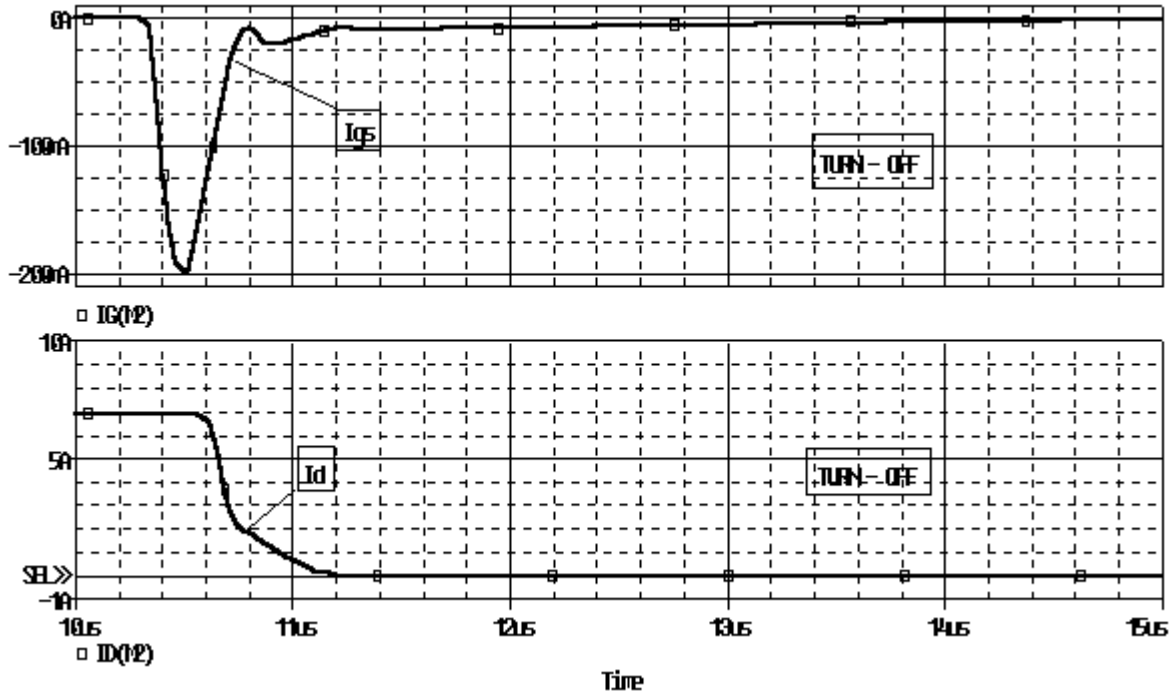

Fig.5

4. CONCLUSION

The principal of active gate control method based on direct sensing of dU/dt is applying and is explained. The characteristics of an optimal driving circuit for

MOSFETS devices have been analyzed. Experimental evaluation of the MOSFET performances has been carried out. Active control of the gate can reduce dI/dt thus improving EMI interference.

2. REFERENCES

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