A PRACTICAL SIMULATION-BASED DESIGN OF CMOS CURRENT REFERENCE BASED ON A WEAK INVERSION OPERATION

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The paper proposes a practical simulation-based approach for design of CMOS current reference based on a weak inversion operation. The goal is to achieve the desired values of output current and specified temperature coefficient and to ensure their minimal sensitivity regarding the technology tolerances. For that purpose a simulation-based procedure that uses the result from analysis of the described circuit is proposed. Because of the existence of countless solutions for transistor dimensions, an optimization loop is implemented in order to find a solution, which has a minimum area. The design methodology is realized by using OCEAN Scripts in Cadence Analog Design Environment, which allows easy transition from one technology to another. The presented design procedure is used to design two current references, produced in 1,0-µm and 0,35-µm n-well CMOS technology. Two types of resistors – one with TC>3000ppm/K, and another with TC<3000ppm/K are used. The developed examples are implemented in real prototypes. The measured results confirm emphatically the proposed approach.

1. INTRODUCTION

The increasing of IC complexity in a shrinking development cycle requires an extensive reuse of intellectual property modules (IP modules) and automated design techniques.

The current references are integrated sub-blocks that find wide application in contemporary analog and mixed-mode circuits. One of the most popular configurations is shown on Fig.1. This circuit uses a single pair of PMOS transistors (M3, M4), operating as a simple current mirror, a single pair of NMOS transistors (M1, M2), working in weak inversion and a resistor R. The value of the resistor is temperature dependent, which determines low temperature stability of the output current. Another drawback of this circuit is its sensitivity regarding the technology tolerances.

The paper proposes a practical simulation-based approach for design of CMOS current reference with enhanced temperature stability and minimal sensitivity regarding the variation of the technology parameters. To this aim the relations between geometrical sizes of the transistors and the output current as well as the results from temperature and tolerance analyses are presented. On this base a method

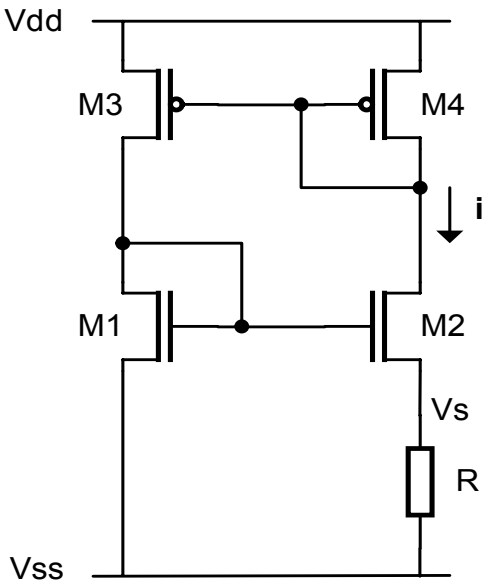

Fig. 1. CMOS Current Reference Circuit Based on a Weak Inversion Operation.

for temperature compensation of the current is discussed and a dimensioning procedure and program are proposed. They are applied successfully in the design of current references through two CMOS technologies.

2. ANALYSIS OF CIRCUIT

When the pair of PMOS transistors (M3, M4) is operating as a simple current mirror in strong inversion and the pair of NMOS transistors (M1, M2) is working in weak inversion, the reference current is:

$$(1) \qquad I = \frac{V_S}{R} = \frac{U_T}{R} \ln\left(\frac{S2}{S1}\frac{S3}{S4}\right),$$

where: $U_T = kT/q$ is the thermal voltage, proportional to the absolute temperature;
S1, S2, S3, S4 are W/L ratios of M1, M2, M3, M4 respectively.

Due to the small value of V_S (40-80 mV at room temperature), a low reference current (less than 1μA) is possible to be generated by using such a value for resistor R that is less than 100kΩ.

If the NMOS transistors operate in strong inversion, the current is equal of:

$$(2) \qquad I = \frac{2}{KP_N \cdot (W_{M2}/L_{M2}) \cdot R^2}\left(1 - \sqrt{\frac{S1}{S2}\frac{S4}{S3}}\right)^2.$$

In the above equation the current I is proportional to the square of the value of resistance R and consequently it is more sensitive to the technology variation in comparison with equation (1). This feature of the circuit forces the use of NMOS transistors that operate in weak inversion.

The temperature coefficient of the output current (TC_I) depends on the thermal voltage U_T and the temperature coefficient of the resistance TC_R. From equation (1) follows:

$$(3) \qquad TC\_I = \frac{1}{I}\frac{\partial I}{\partial T} = \left[\frac{1}{U_T}\frac{\partial U_T}{\partial T} - \frac{1}{R}\frac{\partial R}{\partial T}\right].$$

To obtain temperature independence of current reference (i.e. $TC\_I \approx 0$), the used resistor should have $TC\_R \approx 3300ppm/K$ at room temperature. If the used technology is unable to implement such resistors, two resistors with $TC\_R1 > 3300ppm/K$ and $TC\_R2 < 3300ppm/K$, connected in series ($R = R1 + R2$), can be used. Then the equation for the temperature coefficient of the output current (TC_I) will be:

$$(4) \qquad TC\_I = \frac{1}{(R1+R2)}\left[R1\left(\frac{1}{U_T}\frac{\partial U_T}{\partial T} - \frac{1}{R1}\frac{\partial R1}{\partial T}\right) + R2\left(\frac{1}{U_T}\frac{\partial U_T}{\partial T} - \frac{1}{R2}\frac{\partial R2}{\partial T}\right)\right].$$

The previous two expressions are made on the assumption that the temperature dependence of an integrated resistor is a linear function. In fact resistors' values change in a square law that is usually modeled by a polynomial function in process specifications. Thus, to obtain (3) and (4), only the first coefficient is used.

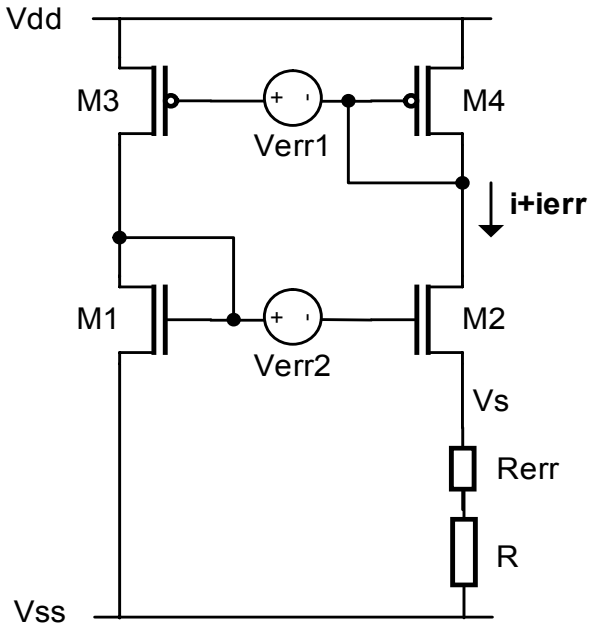

Fig. 2. Circuit for visualization of components that determine the variation of output current.

The values of *TC_I* in equations (3) and (4) depends on the temperature. Consequently, the temperature compensation of the circuit is possible only for concrete values of temperature (for example at room temperature T=300K).

The variation of the reference current regarding the technology is determined by the following components Fig.2 [2, 3]:

- Threshold voltage mismatch *Verr1* in PMOS transistor pair M3-M4. It causes the current error *Ieer1*;
- Threshold voltage mismatch *Verr2* in NMOS transistor pair M1-M2. It causes the current error *Ieer2*;
- The error *Rerr* that is a result from the variation of the resistors' widths *DW*. It causes the current error *Ieer3*.

The current errors *Ieer1*, *Ieer2* and Ieer3 are random, not correlated variables. Consequently, the standard deviation of output current *I* is equals to:

$$(5) \qquad \sigma I^2 = Ierr1^2 + Ierr2^2 + Ierr3^2,$$

where $Ierr1 = f(Verr1)$, $Ierr2 = f(Verr2)$ and $Ierr3 = f(\mathrm{Re}rr)$.

The dependencies of the current errors from both threshold voltage mismatches can be obtained by DC simulation. This is a simple and more precise approach in comparison with the using of complex standard analytical transformations.

Verr1 and *Verr2* are approximately inverse proportionally of the area of the respective transistors. The empirical formulas are:

$$(6) \qquad V_{err1} = \frac{A_{VTP}}{\sqrt{W_P L_P}},$$

$$(7) \qquad V_{err2} = \frac{A_{VTN}}{\sqrt{W_{M1} L_{M1}}},$$

where A_{VTP} and A_{VTN} are technological parameters.

The value of the resistor is determined by its geometrical sizes W and L and by the specific sheet resistance R_{Sh}. The relations are:

$$R \pm \mathrm{Re}\,rr = \frac{R_{Sh} L}{W \mp Werr}. \tag{8}$$

$$W = Werr \left(\frac{1 + \frac{\mathrm{Re}\,rr}{R}}{\frac{\mathrm{Re}\,rr}{R}} \right) \tag{9}$$

In the above formulas *Rerr* is the error of the resistors, and *Werr* is defined as:

$$Werr = \left(\frac{DW\,\max - DW\,\min}{6} \right) * 2. \tag{10}$$

The parameter *DW* (*Delta Width*) is given in the specification of the technological process. It is equal to the difference between the width of the designed resistor and the real produced resistor. *DW* varies between DW_{min} and DW_{max} and has a character of probability.

3. DESIGN PROCEDURE

The generalized block diagram of the proposed procedure for CMOS current mirror dimensioning and optimization is given on Fig.3. It consists of a dimensioning procedure and an optimization cycle. The goal is not only to achieve the value of the output current and the specified temperature coefficient, but also to guarantee their minimal sensitivity regarding the technology tolerances. For that purpose a simulation-based procedure that uses the result from the analysis of the described circuit is proposed. Because of the existence of countless solutions for transistor dimensions, an optimization loop is used, which aims to find a solution with minimum area. Due to this reason, in each step of the dimensioning process, the circuit parameters are extracted and evaluated by simulations until the optimal solution is obtained.

The input information for the presented procedure is:

- the specified value of the output current I_{nom};
- the maximal deviation of the output current $\pm \Delta I$;
- the temperature coefficient of the output current *TC_ I*;
- the value of power supply VDD;
- the technology process data;
- the minimal sizes *W* and *L* of the transistors and the resistors, which are specific for the applied technology;
- the size coefficient *W/L*.

At the first step of the procedure, the initial values of the circuit parameters are calculated by using the specified values of I_{nom} , *TC_ I* and the equations (1) ÷ (10). After that, the sizes of the devices are scaled in order to guarantee the desired maximal deviation of the output current $\pm \Delta I$. In the next step, to enhance the accuracy

of the output current I_{nom}, the procedure provides repetition of some computations and calculations of the circuit area S_i. Its value is the input parameter of the optimization cycle that uses "the golden section" method.

The design methodology is realized by using OCEAN Scripts in Cadence Analog Design Environment, which allows easy transition from one technology to another.

4. PRACTICAL VERIFICATION

The presented procedure is used to design two current references, produced in 1,0-μm and 0,35-μm n-well CMOS technology. Two types of resistors – one with TC>3000ppm/K, and another with TC<3000ppm/K are used. The obtained solutions are applied for implementation of real prototypes. Fig.4 demonstrates the results from the measurements of 20 experimental chips that are manufactured in 0,35μm CMOS technology. The circuits are examined at 1.5V, 2V, 2.5V and 3V power supply.

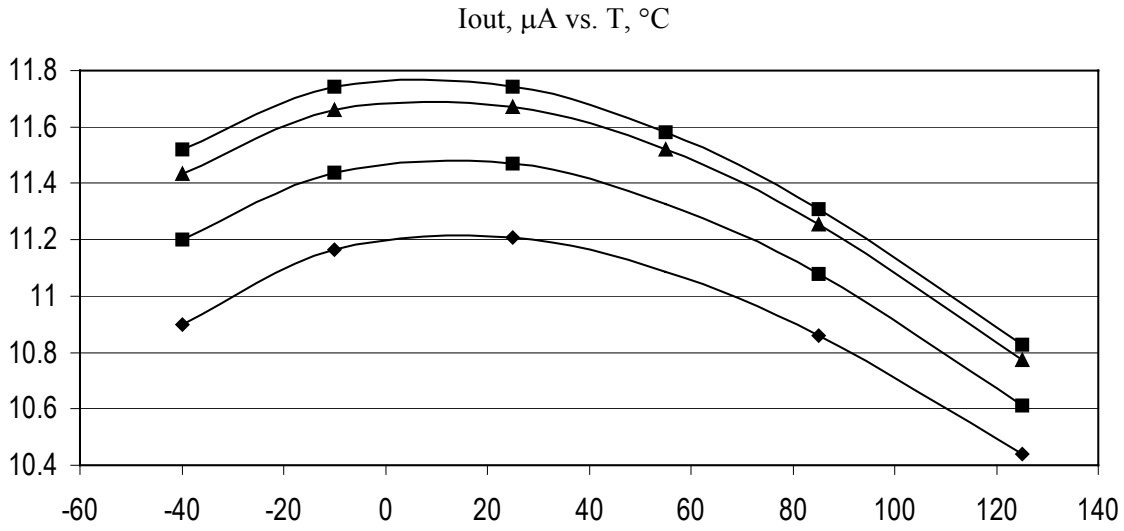

Fig.4. Experimental results from examination of 0,35 μm CMOS current mirror.

5. CONCLUSION

In this paper an analysis of the basic relations in the CMOS current reference circuit, based on weak inversion operation, is carried out and a simulation-based design procedure for its optimal dimensioning is proposed. The procedure is realized by using OCEAN Scripts in Cadence Analog Design Environment and ensures independence from the technology. The procedure is practically examined and the obtained results confirm its effectiveness.

The presented approach will find wide application in the practical design of analog and mixed-mode circuits as well as in the education on microelectronics.

5. REFERENCES

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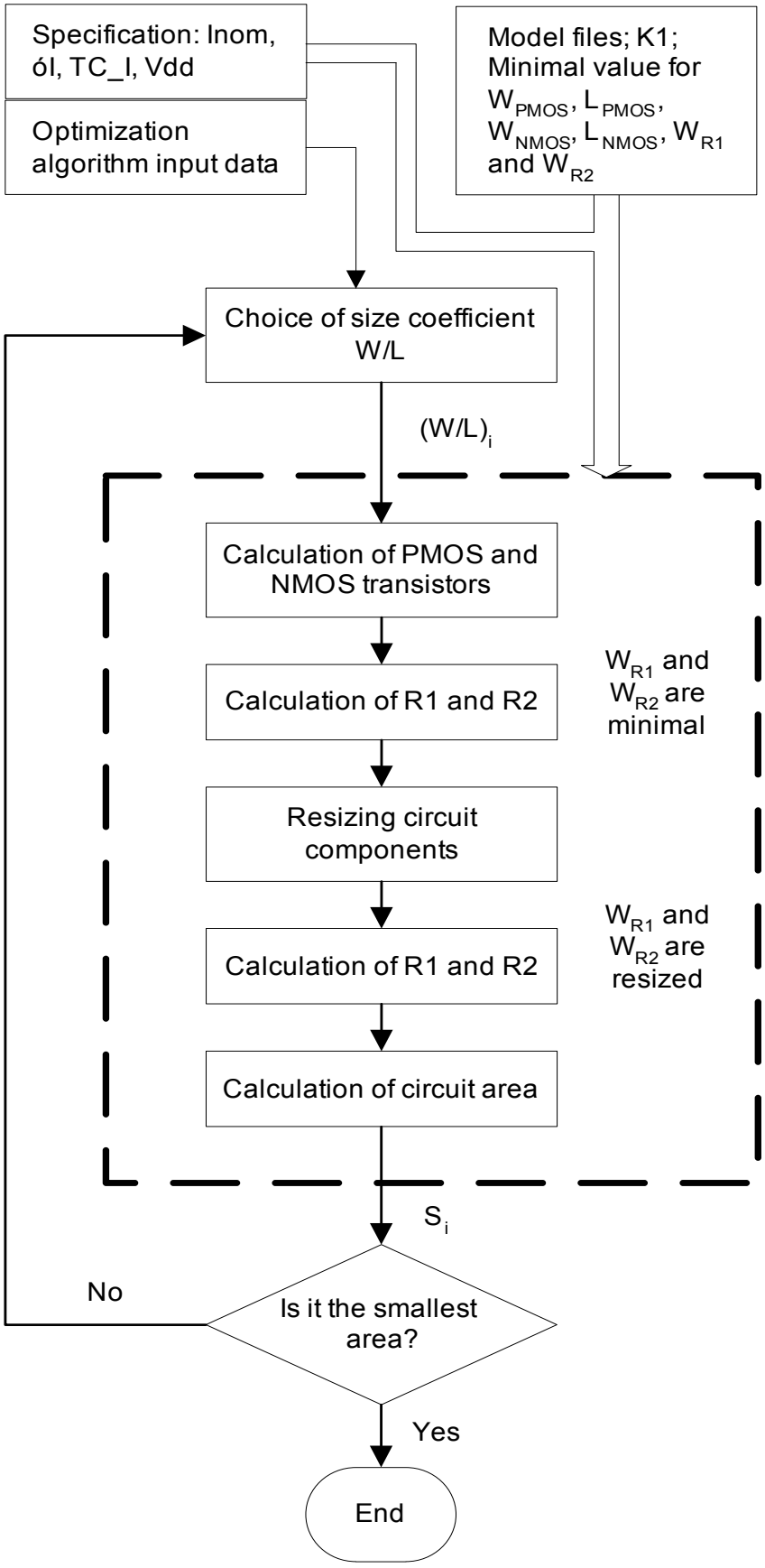

Fig. 3. Block diagram of algorithm for CMOS current reference dimensioning and optimization.