FULLY-INTEGRATED 2.4GHz VCO WITH LOW PHASE-NOISE

Radek Georgiev Nachev, Kolyo Petrov Ivanov, Marin Hristov Hristov, Stefan Yordanov Ovcharov, Anna Stoynova Andonova

ECAD Laboratory, FETT, Technical University of Sofia, 8 Kliment Ohridski Str. 1000, Sofia, Bulgaria, phone: +359 2 965 3115, e-mail: radek@ecad.tu-sofia.bg, kolyo_ivanov@abv.bg

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This paper presents a fully-integrated voltage controlled oscillator working in the 2.45GHz ISM band. It uses the standard differential design as it gives major advantages – high suppression of noise on the power supply lines, better start-up for a given power consumption. The oscillator achieves very low phase noise of -123dBc/Hz at 1MHz offset from the carrier. Emitter degeneration technique is used to improve the phase noise over the standard design. The power consumption of the oscillator is 8mA from a 3V power supply. The output voltage amplitude is 800mV. The tuning frequency range is 2.38-2.68GHz and the tuning voltage is from 2V to 3 V.

1. INTRODUCTION

The 2.4GHz ISM (Industrial, Scientific and Medical) band is used in many standards for wireless communication like Bluetooth, IEEE 802.11b,g and etc. It is estimated that the demand for devices using these standards will continue to increase as our world will continue to become more and more "wireless". The main areas for these devices are wireless LAN, PAN (Personal Area Networks), BAN (Body Area Networks) and etc. For example, since Bluetooth was first officially standardized in 1999, the Bluetooth market has grown to more than 35 million devices per year.

The voltage controlled oscillator is one of the most important blocks of the transceivers and it determines the overall performance of the system. This is especially true for the noise performance – transceivers should meet stringent noise requirements while keeping the power consumption low. These two requirements are contrary to each other, and there is always some trade-off between them.

This paper presents a VCO design using the SiGe HBT (Hetero-junction Bipolar Transistor) module from the 0.35um BiCMOS technology of Austriamicrosystems AG, Austria. In the design special attempts have been done to reduce the phase noise while keeping the power consumption at the same level.

1. SCHEMATIC DESIGN OF THE VCO

1.1 Basic schematic description.

The VCO schematic is given on Fig.1. It uses the differential design because it has major advantages - suppression of the noise on the supply lines as it appears as a common mode signal at the differential output. Also the differential circuit allows for a better start-up of the oscillator because of the strong positive feedback in the loop of the transistor differential pair. Single-transistor VCO like Colpitts for example would typically need higher bias currents and higher consumption to achieve the same start-up as the differential VCO.

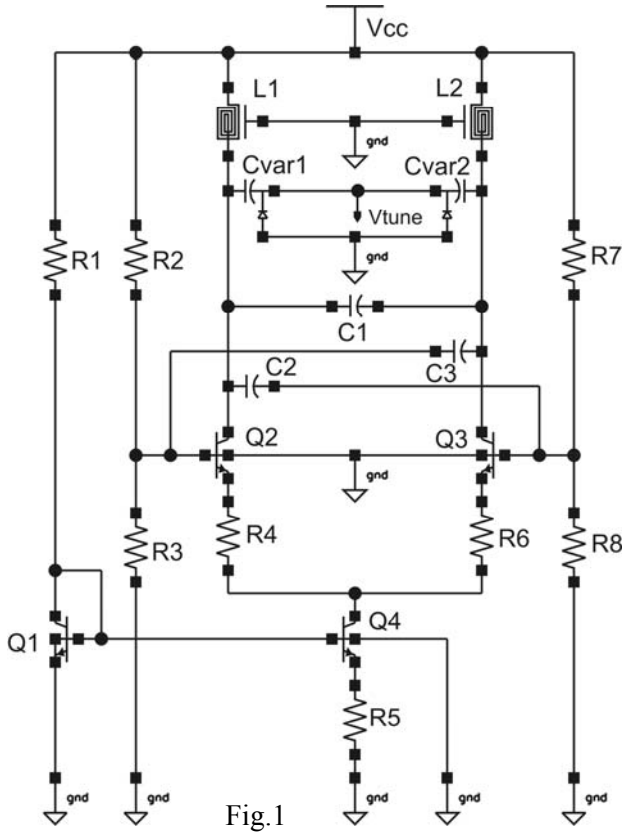

Fig.1

The differential pair consists of the transistors Q_2 and Q_3. The feedback signal is taken from each collector and supplied to the base of the other transistor. The capacitors C_2 and C_3 separate the DC bias potentials of the bases and collectors of Q_2 and Q_3. The LC resonator consists of the inductors L_1 and L_2, capacitor C_1 and the varactors C_{VAR1} and C_{VAR2}. The resistors R_1, R_2, R_3, R_7, R_8, and transistors Q_1 and Q_4 establish the bias point of the oscillator.

The emitter degeneration technique for decreasing the phase-noise is implemented using the resistors R_4, R_5, R_6.

1.2 Design parameters of the schematic components.

The design parameters of all schematic components are given in Table 1. The transistors Q_1, Q_2, Q_3, and Q_4 are SiGe HBT transistors with f_T=60GHz. The inductors L_1 and L_2 are on-chip inductors with Q=9 at 2.4GHz. The varactors C_{VAR1} and C_{VAR2} are technology given MOS varactors with Q=60 at 2.4GHz. The capacitors C_1, C_2, C_3 are MIM (Metal-Oxide-Metal) capacitors with excellent high-frequency behavior.

Table 1
Design parameters of the schematic components

component	value	component	value
V_{cc}	3V	R_3,R_8	4kΩ
V_{tune}	(2÷3)V	R_4,R_6	30Ω
Q_2 , Q_3	area = 0.4x10μm^2	R_5	11Ω
Q_1	area = 0.4x1μm^2	C_1	1pF
Q_4	area = 0.4x6μm^2	$C_{VAR}1_{max}$,$C_{VAR}2_{max}$	1.75pF at V_{tune}=2V
R_1	1.2kΩ	C_2,C_3	2pF
R_2, R_7	2kΩ	L_1,L_2	1nH,Q=9 at 2.4GHz

2. SIMULATION RESULTS

2.1 Effect of the emitter degeneration on the phase noise.

The effect of the emitter degeneration on the phase noise is shown on Fig. 2. We can see that addition of emitter degeneration resistor R_5 in the tail transistor Q_4 improves the phase noise with approximately 3dB – from 110dBc/Hz to 113dBc/Hz. Addition of resistors R_4 and R_6 further improves the phase noise with additional 3dB, and the final phase noise is 116dBc/Hz. This example show that using the emitter degeneration technique we can significantly improve the phase noise and move the

circuit from a point where it hardly satisfies the standard requirements (-110dBc/Hz at 1MHz offset for Bluetooth for example) to a very good compliance with the standard.

In order evaluate the effect of emitter degeneration the bias point of the oscillator for the three cases was slightly adjusted through resistor R_1. This is necessary to keep constant the current of the tail transistor Q_4 and this way to keep constant the output signal amplitude. Phase noise is a ratio between the output signal power and the total noise power at the output. Any increase of the output signal amplitude at the cost of higher consumption (higher tail current) will improve the phase noise because the total noise power at the output is relatively constant.

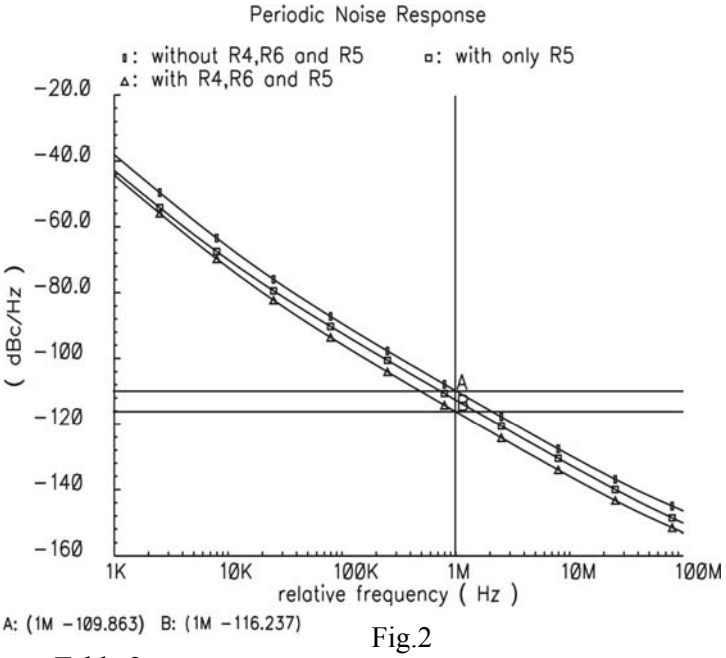

Fig.2

Table 2

		no emitter degeneration V^2/Hz	with R_5, V^2/Hz	with R_5 and R_4, R_6, V^2/Hz
Q_1	rbx	8.64e-13	2.84e-13	9.93e-14
Q_1	rbi	3.59e-13	6.94e-14	2.42e-14
Q_4	rbi	3.32e-13	1.36e-13	4.46e-14
Q_4	itzf	2.55e-13	1.75e-13	4.80e-14
Q_1	re	1.81e-13	6.63e-14	2.26e-14
Total		2.98e-12	1.43e-12	6.08e-13

The simulator SpectreRF from the Cadence environment gives possibility to print-out the contributions to the total output noise of every noise source in the circuit. The print-out for the first 5 biggest contributors is given in Table 2. We can see that the main noise contributors are the transistors in the current mirror Q_1 and Q_4 that set the bias point. The design kit of the technology uses the VBIC (Vertical Bipolar Inter-Company) model of the bipolar transistors and we see that basically the base resistances of these transistors contribute the main part of the noise. We can make the conclusion that the improvement of the phase noise with emitter degeneration is due to the reduction of the gain factor of the transistor Q_4 which is common-emitter gain stage for the noise sources of the base resistances. The total effect of the emitter degeneration is decreasing the phase noise to one half and consequently to one fourth of the starting value. This means that the phase noise decreases with 3dB and 6dB respectively.

2.2 Tuning range.

The tuning range of the oscillator is from 2.38GHz to 2.69GHz with tuning voltage V_{tune} from 2V to 3V (Fig. 3). It fully covers the frequency range of Bluetooth and IEEE 802.11 standards – 2.4-2.4835GHz. We can see two almost linear regions of the frequency tuning range – one in the region for V_{tune}=2-2.5V, with tuning constant K_{VCO}=90MHz/V approximately, and the other for V_{tune}=2.6-3V with

K_{VCO}=600MHz/V. This behavior of the tuning range is determined by the C-V curve of the MOS varactors given in the technology.

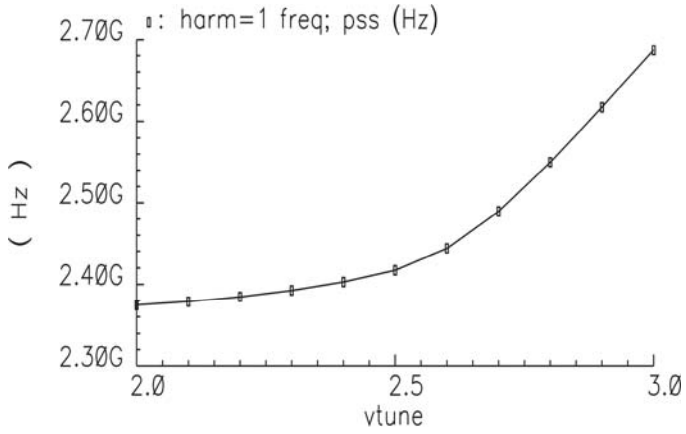

Fig.3

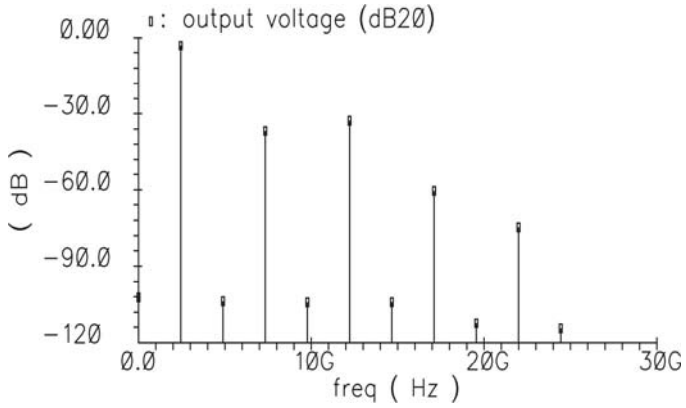

Fig.4

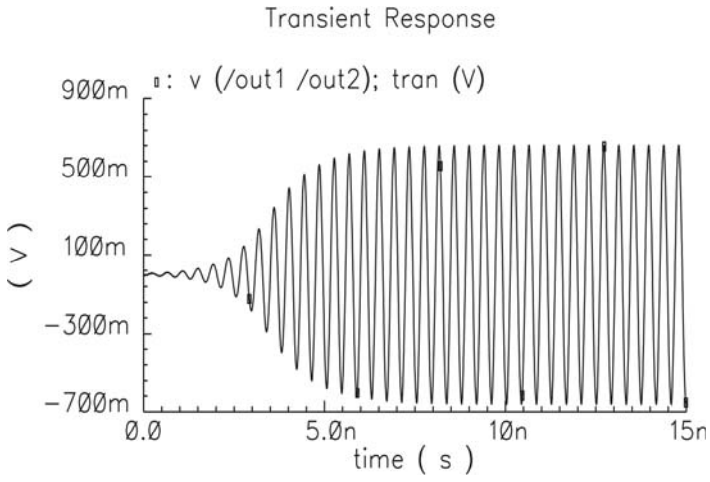

Fig.5

2.3 Linearity of the output signal.

The output voltage amplitude is 700mV. The output voltage is highly linear as can be seen on Fig.4. The high linearity is mainly determined by the quality factor of the LC tank which is approximately Q_{tank}=7. The relatively high quality tank filters the higher order harmonics and only the first harmonic is dominating the output. The second largest harmonic (fifth order harmonic) is approximately 30dB smaller than the first harmonic.

2.4 Oscillator start-up and power consumption.

One of the main targets of the design is to achieve reliable start-up while maintaining the power consumption low. These two conditions are contrary to each other because the reliable start-up requires high bias current in order that the transistors Q_2 and Q_3 of the differential pair have high transconductance g_m. In our case a trade-off between the two conditions gave collector currents I_c=2.6mA for the transistors and a total power consumption of approximately 8mA from a 3V power supply. The start-up output voltage waveform is given on Fig. 5.

3. PHISICAL DESIGN OF THE OSCILLATOR

3.1 Oscillator layout

The oscillator layout is given on Fig.6. The layout dimensions are 900x700μm^2. After resimulation of the circuit the tuning range shifted down with approximately 300MHz. It is due to the fact that parasitic capacitances of metal layers overlap added in parallel with the LC tank. In order to correct the tuning range, the capacitance C_1 was decreased with 0.2pF and thus the tuning range returned to its previous values. The decrease of C_1 affected the

phase noise which increased to 123dBc/Hz at 1MHz offset from the carrier. The phase noise versus frequency offset is given on Fig.7. The output voltage amplitude increased to 800mV. It shows very good linearity, the second largest harmonic is 34dB below the first harmonic. The harmonic content of the output voltage is given on Fig.8. The current consumption increased to 8.5mA. The final frequency tuning range is 2.38-2.68GHz and is given on Fig.9. The tuning constant remains the same - K_{VCO}=90MHz/V for the region V_{tune}=2-2.5V, and K_{VCO}=600MHz/V for the region V_{tune} =2.6-3V.

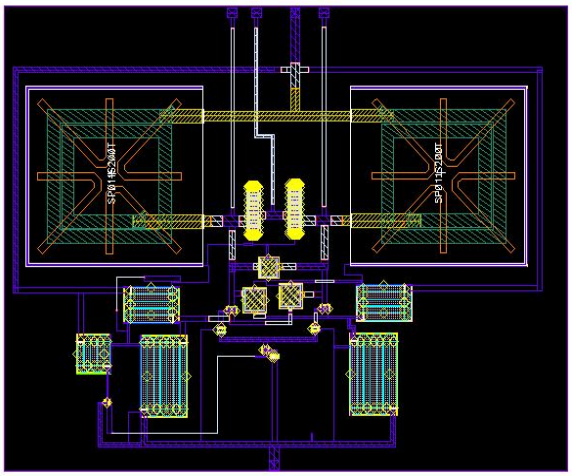

Fig.6

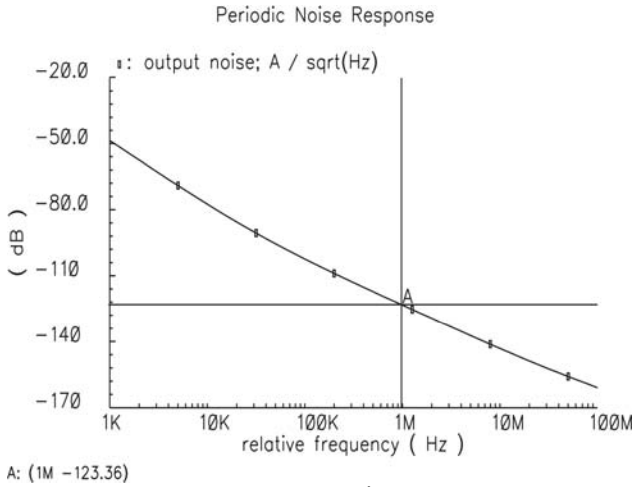

Fig.7

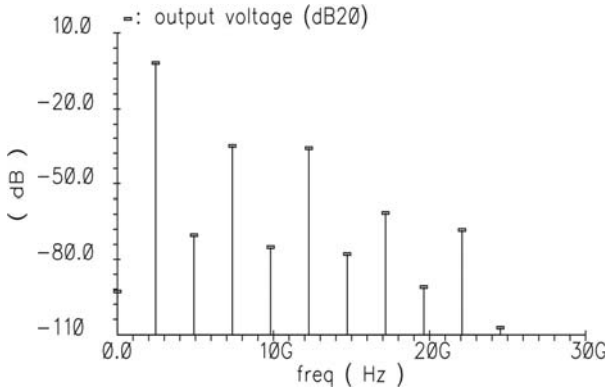

Fig.8

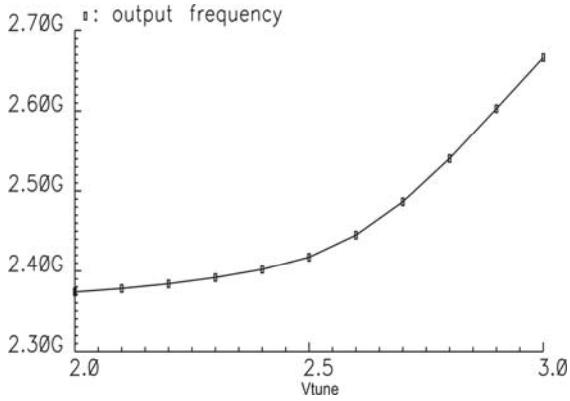

Fig.9

4. CONCLUSIONS

This paper presents top-down design of VCO oscillator for wireless communication standards like Bluetooth and IEEE 802.11. The VCO is designed with 0.35um HBT BiCMOS technology and achieves very low phase noise -123dBc/Hz at 1MHZ offset and low power consumption – 26mW. The tuning range of the VCO fully covers the ISM frequency band 2.4-2.4835GHz used by these standards. The output voltage amplitude is 800mV.

5. REFERENCES

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