SiGe HBT: TECHNOLOGY AND PARAMETERS- FREQUENCY RESPONSE AND CURRENT GAIN

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1. INTRODUCTION

The technological and design parameters of the heterojunction bipolar transistors with SiGe base (SiGe HBTs) have been investigated [1].

The special features of SiGe HBT (polySi emitter, internal/external epi-base very often with in-situ doping, typical concentrated profiles of the impurity and Ge self aligned structure, etc) lead to improve frequency properties and high, in some cases too high values of h_{FE}.

The present article treats the two main parameters of SiGe HBT;

The cut-off frequency f_T very characteristic dynamic parameter of UHF transistors, determine the possibilities for their usage in UHF applications and the current gain parameter h_{FE}, is included evidently in f_T parameter and indicating for the specific type of transistors the optimal Gumel-number of the emitter and the base and allowing the HBT designer to improve their characteristics, including their noise properties by means of profile optimization of the doped impurity in the internal base. Information is given about the influence of the vertical scaling upon the quick-action of UHF transistor with extreme narrow active base.

2. MAIN SECTION

From the middle of the 80-s to the middle of the 90-s propagation delay time t_{pd} of the emitter coupled logic (ECL) valves, prepared with SiGe HBT was reduced about 5 times. For that purpose the following technologies were designed and put into production:

-Self aligned bipolar technology with double polisilicon–SABT;
-Technology of the deep isolating trench –TIT;
- Shallow junctions formation technologies (SJFT).

In 1992, t_{pd} = 20 ps was achieved using epitaxial SiGe base. For very high-speed VHF applications – the optical fiber communication systems for example, especially high-speed transistors are needed. The improvements of the frequency performances are obtained by the aid of:

-Vertical scaling – directly improves f_T;
-Horizontal scaling – decreases C_{TC} (C_{cb}) and r_{bb}.

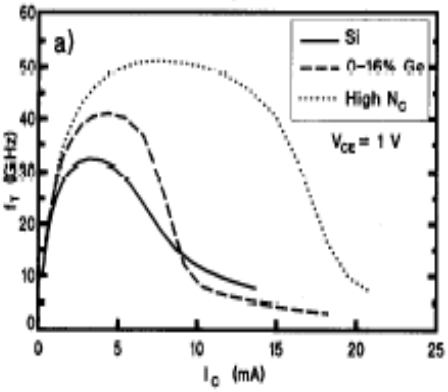

Figure 1 (The relation $f_T = f(N_{GE})$)

It has been pointed out [1] that the inclusion of aiding field (Ge in the base of the transistor) increases f_T. The relationship $f_T = f(N_{GE})$ is seen from Fig.1:

The augment of N_{GE} leads to the increase of f_T.

The cut-off frequency f_T of HBT SiGe base is apparently higher than that of the classic bipolar Si transistor in the range of a medium current, while at high-doped collector ($N_C = 1{,}7.10^{17}$ cm^{-3}) that difference is very well expressed in the middle and high levels of I_C.

The explanation of this effect lays in the controlled deformation of the base [1]. At the arise of dislocations of discrepancy with high density (exceeding the critical thickness), the deformation of SiGe layer is relaxed, which leads to the loss of mearly 0,5 ΔE_g and the aiding field decreases, τ_b increases correspondingly.

At high values of I_C the electrons concentration exceeds the space charge and the quasineutral base widens (effect of Kirk) and when it passes behind the end of SiGe layer, a potential barrier is formed, which is a hindrance for the transportation of the current carriers, decreases h_{FE} and increases t_f;

At $I_C > 9$ mA, f_T of HBT with SiGe base is lower in comparison with that of Si transistor, i.e. SiGe transistor has advantage in speed over Si transistor only in a definite range of the collector current (J_C – more precisely), namely in junction area low-medium and medium collector currents, for which it finds application, in unsaturated digital integrated circuits (IC), (ECL for example) and low signal analog IC. The rapid decrease of f_T at high values of Jc can be compensated to a certain extent by:

Enlargement of SiGe more inwards the collector (but increasing the thickness of SiGe layer, it can change from stable to pseudo stable).

Increasing the doping of the collector (see the dotted curve on Fig.2), which definitely improves the transistor's frequency characteristics at the expense of lower breakdown voltages BU_{CBO} and BU_{CEO} and augmented values of C_{TC}.

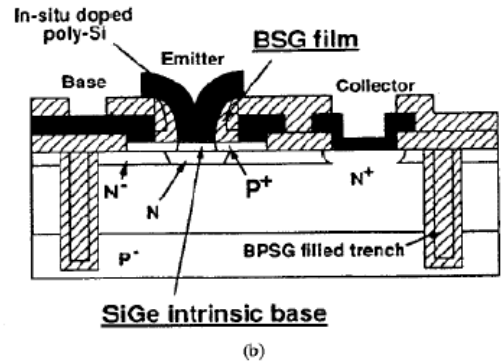

Figure 2

On Fig 3 is shown the relation $f_T = f(U_{CEO})$ for transistors with Si and SiGe base. It is seen that increasing the U_{CE} the transient frequency decreases.

It is proved by theory (2) that the upper limit of the product $f_T.BU_{CEO}$ is constant, depending on the semiconductor material. For transistors with Si base the value of the product $f_T BU_{CEO}$ is as follows:

$f_T BU_{CEO} = 200$ v.GHz (1)

When the duration and temperature of the processes after epi-laying of SiGe layer

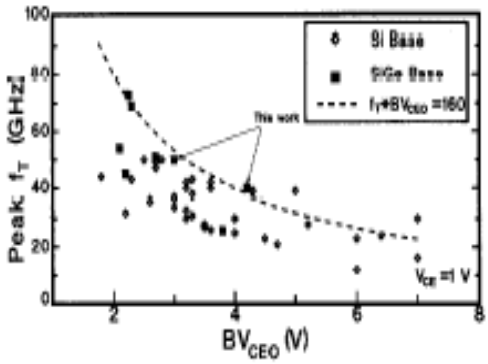

Figure 3

(Applying small thermal budget) are properly selected then no characteristics degradation is seen at SiGe HBT as a result of the rise of dislocations of discrepancy and relaxation of the deformed SiGe base.

In view of the fact that the introduction of Ge in the base of such transistors does not influence upon their short-term and long-term reliability, which means that the controlled deformation of the base layer can be used for improving the high speed of the transistors.

From the beginning up to the middle of the 90-s the possibilities for further improvement of the transistors frequency characteristics by means of scaling decreased, because of the following reasons:

-The further vertical scaling becomes problematic, because the higher f_T has as a concomitant effect high r_{bb}, as a result of thin internal base, which leads to a compromise between f_T and r_{bb};

-The horizontal scaling gets more complicated, because of h_{FE} decreases as a result of the narrow emitter effect, known as emitter plug effect at sub micron width ($W_E < 0{,}5$ μm) of the emitter (3)

The problem was smartly solved (4) by the combination of rapid vapor-phase doping (RVD) of the base, which leads to higher f_T and low resistance of the base r_{bb}, and the decrease of current gain is suppressed by using in-situ phosphorous doped polysilicon (IDP) and with IDP technology the r_C of devices with small emitters, can even be decreased.

The high performances are result of the application of shallow junction formation technology (SJFT). RVD method for base forming is a method of diffusion from vapor phase (800^0 C, 15 min, for example), while the boron profile forms steep junction without channelling, (because the ion induced defects of the ion implantation are missing) which is why this method is appropriate for the forming of thin step base with high concentration of the impurity. In IDP method the emitter is formed by diffusion in-situ phosphorous-doped layer of amorphous silicon, which is laid at low temperatures (520^0 C) of Si_2H_6 and PH_3. IDP method is suitable for decreasing the thermal budget and r_e. The phosphorous atoms can be ionized even at low temperature annealing (LTA) at $t^0 = 650^0$ C.

The structure of RVD ÷ IDP Si transistor (briefly IDP transistor),[4] is with homotaxial base structure, but the silicon base can be easily changed with SiGe base with the priorities of the aiding field introduction. It's the most important advantages are three:

-Base with steep profile of the impurity;

-Emitter, formed with highly doped polySi;

-Highly decreased active collector area by the help of pedestal collector implantation for the purpose of suppressing the Kirk effect and very thin (0,4 μm) epitaxial layer. In spite of the higher collector doping and its very small thickness BU_{CEO} = 2,4 v is achieved, which is sufficient for most applications.

DC and AC parameters of IDP are shown in table 1and compared with these of a conventional Si UHF transistor with polySi emitter implanted with as.

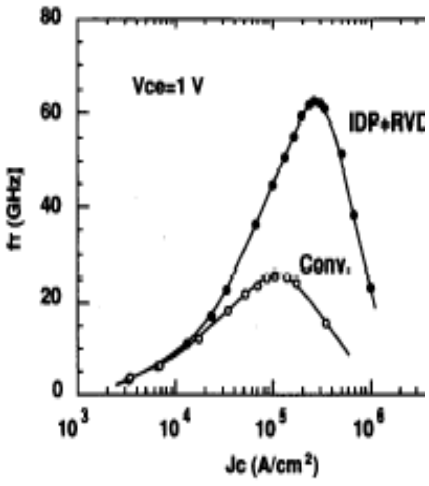

Figure 4

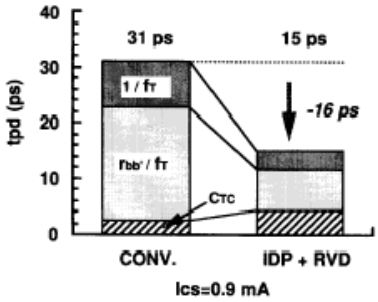

Figure 5a

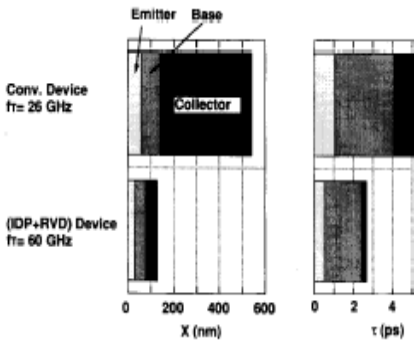

Figure 5b

It is observed the 5 fold higher current gain; over the 2,5 fold higher f_T, the 3 folds lower r_e of IDP ÷RVD transistor and a little higher values of C_{TC} and C_{TE}.

The relation $f_T = f(J_{C)\ is}$ shown on Fig. 4, both for the IDP and the conventional transistor. The difference in f_{Tmax} is obvious and here in contrast to Fig.2 the supremacy of IDP transistor is valid even at high values of Ic.

The delay time t_{pd} of ECL valve, consisting of IDP transistor with S_E = 0,3 x 1,1 μm is record low (t_{pd} = 15 ps at Ics = 1,2 mA), while t_{pd} of the conventional transistor is t_{pd} = 32 ps. At higher values of the switching current, t_{pd} depends mainly on f_T, r_{bb}, C_{TC} (see Fig. 5 a and b).

On Fig. 5 as is seen, that the vertical scaling of IDP transistor concerns all active areas – the two fold decrease of X_{JE} and the width of the active base W_B, but the main scaling is in the active collector area – 8 orders decrease of the collector thickness.

TABLE I
MEASURED DEVICE PARAMETERS OF THE FABRICATED TRANSISTORS

Device		IDP+RVD	Conv.
Emitter Area	A_E (μm²)	0.4x1.1	0.3x1
Current Gain	h_{FE}	600	120
C-E Breakdown Voltage	BV_{CEO} (V)	2.4	3.7
Early Voltage	V_A (V)	10	18
E-B Capacitance	C_{TE} (fF)	2.7	2.2
C-B Capacitance	C_{TC} (fF)	2.4	1.6
Emitter Resistance	R_E (Ω)	15	45
Base Resistance	$R_{bb'}$ (Ω)	380	380
Pinched-Base Sheet Resistance	R_{bi} (kΩ/□)	35.7	16.2
Cut-Off Frequency	f_t (GHz)	63	25
	f_{max} (GHz)	52	40

On Fig.5 b one can see that the main component, influencing on the difference of t_{pd} (IDP) towards the conventional transistor, is f_T – by the aid of the members 1/ f_T and $r_{bb'}/f_T$ (C_{TC} is 1,5 fold higher in value, see table 1). The higher f_T on its part is due to the decrease of W_B and the collector thickness.

Rather high values of h_{FE} (of the order 600) are suitable for improving the transistor's characteristics by base profile optimization.

The pointed out technological process, implemented in SJFT are perspective for UHS MOS VLSI Ics.

3. CONCLUSION

1. The influence of germanium inclusion in the base of Si bipolar transistor upon the transistor transient frequency f_T is described in the present article, as well as the relation $f_T = f(Ic)$, determining the advantage of high speed of SiGe HBT over Si BJT in limited current range.

2. Attention is paid to the possibility of transistor's frequency improvement by changing the concentration of the impurity in the collector and shifting the Ge-concentrated profile along the length of the active base.

3. One of the main problems of SiGe HBTs with submicron width of the emitter (plug of the emitter) is considered as well as its possibility for elimination by the help of IDP emitter, so called (IDP +RVD) transistor.

4. The main advantages of the IDP transistor over the conventional Si BJT – one with polySi emitter are shown graphically as regards to f_T and the influence of the vertical scaling upon t_{pd} of ECL valve, made of IDP transistors, which can be easily transformed into UHF transistors with SiGe base.

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