

THE INFLUENCE OF GEOMETRY AND TEMPERATURE ON THE PARAMETERS OF INTEGRATED RESISTORS

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B. Sc. M. K. Galionova, M. Sc. D. Pukneva, Assoc. Prof. Ph. D. M. Hristov: "The influence of geometry and temperature on the parameters of Integrated Resistors" is discussed. The value of every integrated resistor depends on its geometry, sheet resistance and temperature. In this paper is examined the influence of the geometry on the basic parameters of the polysilicon (polySi) resistors utilizing the computer-aided design system CADENCE. The influence of the temperature on the resistors parameters and its stability is also studied. Comparison between ideal, modeled and extracted resistors is made. AMS 0.35 μ m SiGe BiCMOS technology is used. The polysilicon resistor is chosen to be studied, because it has small parasitic capacitance, low temperature coefficient and compact structure.

1. INTRODUCTION

Integrated resistors are divided into five groups, depending on the structure: diffusion, epitaxial, pinched, ion-implanted and polysilicon resistors.

Traditionally, resistors are single crystal silicon (Si) or polysilicon (polySi) made from implants and layers already existing in the process (e.g. gate poly). This simplifies the process but makes it more difficult to optimize separate parts of the process. For example, changing the polysilicon deposition technique, may change the polycrystalline structure and the resistance value of the resistors. Single crystal resistors tend to have larger parasitic capacitance and larger voltage coefficients and are therefore less attractive than polysilicon resistors.

Polysilicon resistors are available in CMOS and BiCMOS processes. The polySi used for constructing MOS gates is heavily doped to improve conductivity and has a sheet resistance from 25 to 50 Ω/\square . Poly resistors are resided on top of field oxide. This not only reduces the parasitic capacitance between the resistor and the substrate but also ensures that oxide steps do not cause unexpected resistance variation. If the parasitic capacitance of the field oxide is still too large for a given application, consider using a second poly layer (if available) since the interlevel oxide will further reduce the parasitic capacitance. Reducing the tolerance of the polysilicon resistors may be achieved by carefully controlling the polysilicon thickness, the deposition process, the implant dose, and finally the thermal cycle, including lower temperature interconnect processes which may cause inactivation of dopants. The lower the sheet resistance the easier the polysilicon resistor is to control. For these reasons, polysilicon resistors rarely have tolerances less than 15%.

2. ANALISYS OF POLYSILICON RESISTORS “RPOLY2”

The influence of geometry and temperature on the basic parameters of the polySi resistor “rpolym2” is examined, utilizing the computer-aided design system CADENCE. In Fig. 1. is shown the model, which is used for the investigation of the polySi resistors. It is built of two ideal resistors – R_1 and R_2 , and three ideal capacitors – C_{S0} , C_{S1} and C_M .

$$R = R_1 + R_2 \quad R_1 = R_2 = \frac{1}{2} R$$

$$C_{S0} = C_{S1} = \frac{1}{4} C \quad C_M = \frac{1}{2} C$$

Where R is the total resistance and C is the distributed capacitance. The scheme of connection, which is used for made examines is show of Fig. 1

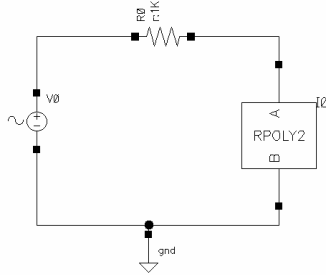


Fig. 1. Scheme of connection on polysilicon “rpolym2”

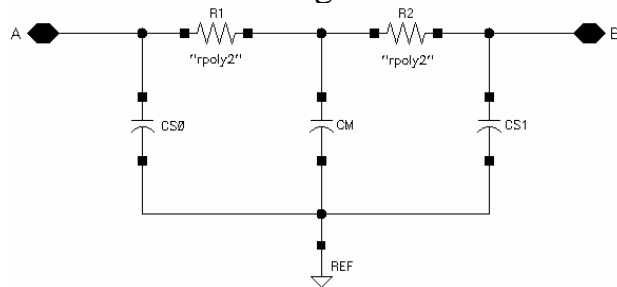


Fig. 2. Polysilicon resistor model

2.1. Influence of the layout

The studies of the influence of the geometry are made for different widths of the resistor ($W = 2 \mu\text{m}$, $W = 6 \mu\text{m}$ and $W = 20 \mu\text{m}$) and different bend (rectangle bend or bend at 45°). Layout on the polysilicon resistor “rpolym2” with width $W=2\mu\text{m}$, value $R=1\text{k}\Omega$ and bends at 90° is show of Fig. 1., and with bends at 45° of Fig. 2.

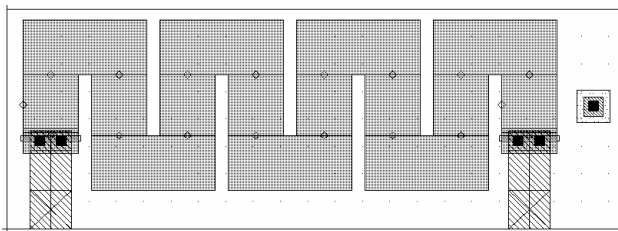


Fig. 1. Layout on the polysilicon resistor “rpolym2” with bends at 90°

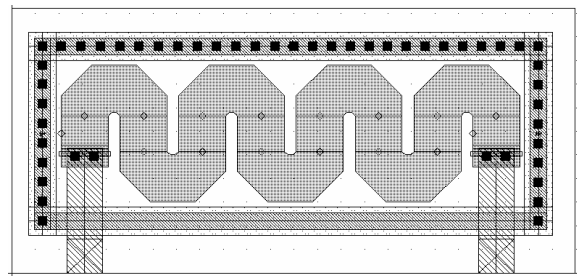


Fig. 8. Layout on the polysilicon resistor “rpolym2” with bends at 45°

2.2. Influence of the temperature

The value of every integrated resistor depends on temperature in a complex, nonlinear manner. Like any nonlinear function, this one can be expanded into a polynomial series. Unless considerable accuracy is required or the temperature varies widely, only the first two terms of the series are significant

$$R(T) = R(T_0) [1 + 10^{-6} T_{CI} (T - T_0)] , \quad (1)$$

where $R(T)$ is the resistance at the desired temperature T ; $R(T_0)$ is the resistance at some other temperature, T_0 ; and α_1 is the linear temperature coefficient of resistivity (TRC) in parts per million per degree Celsius (ppm/°C). A factor of 10^{-6} has been inserted into equation (1) to balance the units involved.

The influence of the temperature on the polysilicon resistor “rpoly2” parameters and its stability is studied for the temperature range $-50 \div 150^\circ\text{C}$.

Comparison is made between ideal resistor, polysilicon resistor “rpoly2” model and extracted view of the resistor, created in CADANCE.

3. RESULTS OF ANALYSIS OF POLYSILICON RESISTORS “RPOLY2”

AC analysis is used to examine the influence of the geometry on the basic parameters of the polySi resistor “rpoly2” and temperature analysis to examine the influence of the temperature on the resistors’ parameters.

3.1. Results of analysis of the layout

Some of the results from the AC analysis are shown in Fig. 1a and Fig. 1b. The analysis is made for resistor widths – 2 μm , 6 μm and 20 μm , and different resistor forms. Resistor’s bends are at 45° or 90° .

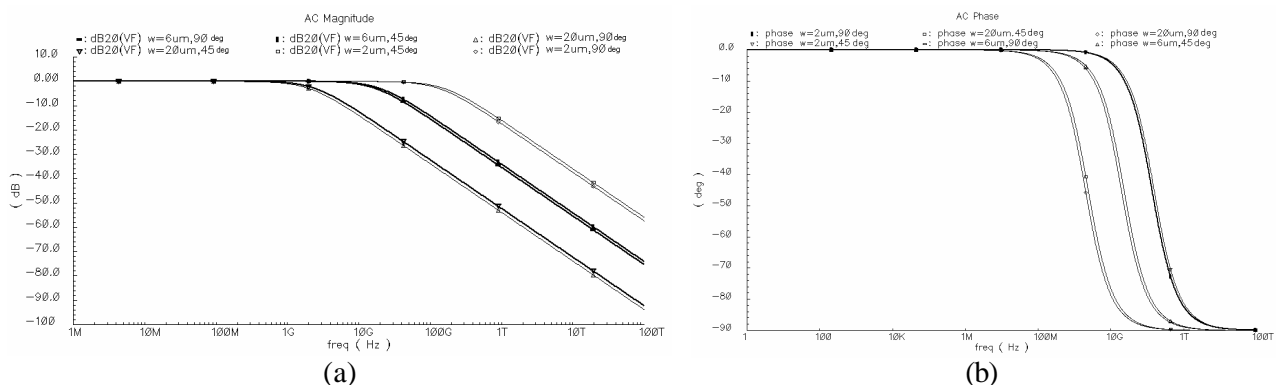


Fig. 3. Frequency response – magnitude (a) and phase (b), for different value of width and different bends (at 45° and 90°)

Parasitic capacitance and parameters of the polySi resistor “rpoly2” in dependence of geometry and form of bends on polySi resistor “rpoly2” are shown in table 2, 3 and 4.

Table 1

Parameters of polySi resistor “rpoly2”	W, [μm]	2	2	2	2
	R, [Ω]	998.6	1003	998.6	1003
	L, [μm]	34.95	35.1	34.95	35.1
	C, [fF]	13.67	16.89	13.67	16.89
Parasitic capacitance	C ₁ , [fF]	0.9507	0.9507	1.562	1.538
	C ₂ , [fF]	0.9507	0.9507	1.562	1.538
Angle of bends, [$^\circ$]		45	90	45	90
Presence of guard ring		no	no	yes	yes

Table 2

Parameters of polySi resistor "rpol2"	W, [μm]	6	6	6	6
	R, [Ω]	1001	1001	1001	1001
	L, [μm]	115.1	115.1	115.1	115.1
	C, [fF]	106	128.8	106	128.8
Parasitic capacitance	C ₁ , [fF]	2.85	2.85	3.069	3.067
	C ₂ , [fF]	2.85	2.85	3.071	3.069
Angle of bends, [$^\circ$]		45	90	45	90
Presence of guard ring		no	no	yes	yes

Table 3

Parameters of polySi resistor "rpol2"	W, [μm]	20	20	20	20
	R, [Ω]	999.9	1000	999.9	1000
	L, [μm]	395	395.1	395	1.33
	C, [pF]	1.099	1.33	1.099	16.89
Parasitic capacitance	C ₁ , [fF]	8.313	8.313	8.564	8.502
	C ₂ , [fF]	8.313	8.313	8.564	8.502
Angle of bends, [$^\circ$]		45	90	45	90
Presence of guard ring		no	no	yes	yes

3.2. Results of analysis of the temperature

Results of the temperature analysis are show at Figure 3 and 4. The analysis is made for width of the resistor $2\mu\text{m}$, $6\mu\text{m}$ and $20\mu\text{m}$, and different form of it (bends at 45° and 90°). The influence of temperature for the temperature range $-50 \div 150^\circ\text{C}$ on the voltage on the resistor is also studied. Results of this examination are show in table 4.

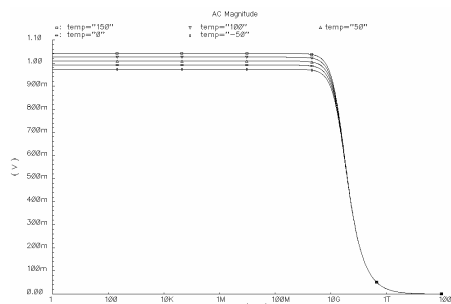


Fig. 4. AC magnitude for different value of the temperature

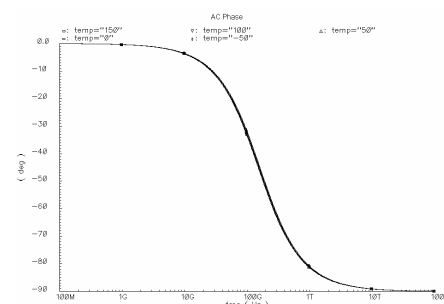


Fig. 5. AC Phase for different value of the temperature

Table 4

Temperature, [$^\circ\text{C}$]	W=2 μm		W=6 μm		W=20 μm	
	45 $^\circ$ bends	90 $^\circ$ bends	45 $^\circ$ bends	90 $^\circ$ bends	45 $^\circ$ bends	90 $^\circ$ bends
150 $^\circ\text{C}$	1,041V	1,043V	1,042V	1,042V	1,041V	1,041V
100 $^\circ\text{C}$	1,024V	1,026V	1,025V	1,025V	1,025V	1,025V
50 $^\circ\text{C}$	1,007V	1,009V	1,008V	1,008V	1,008V	1,008V
0 $^\circ\text{C}$	989,7mV	991,9mV	990,9mV	990,9mV	990,4mV	990,6mV
-50 $^\circ\text{C}$	971,6mV	973,7mV	972,8mV	972,7mV	972,2mV	972,4mV

3.3. Comparison Results

Results of the comparison between ideal, model of the polysilicon resistor “rpoly2”, which is situated in CADANCE and extracted resistors are show at Fig. 5.

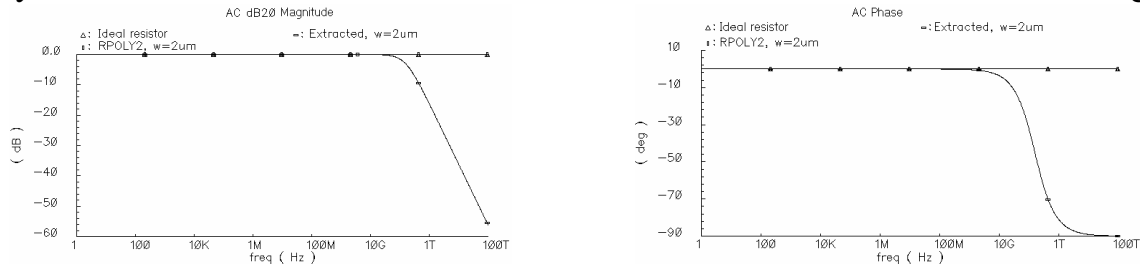


Fig. 4. Resistor Comparison Result

4. CONCLUSIONS

From the polysilicon resistor “rpoly2” study utilizing the computer-aided system CADENCE the following conclusion can be made:

- With the increase of the width of polysilicon resistor, its frequency band becomes narrower.
- The form of polysilicon resistors has an influence on its frequency band. Resistor with bends at 45° has small frequency band width in comparison with rectangle bends resistor with the same width.
- Parasitic capacitance depends on the width of resistor and the size on metal connection. When resistors width is increased, parasitic capacitance value rise, but they remain in the same order.
- Guard ring has influence on the parasitic capacitance. Resistors, which are roundabout with guard ring have bigger parasitic capacitance in comparison with resistors without guard ring.
- Parasitic capacitance does not depend on the resistors form (rectangle bends, bends on 45 degrees), when the resistor is surrounded with guard ring. Parasitic capacitance is the same for bends at 45° and 90° .
- Temperature dependence on the polysilicon resistor “rpoly2” is linear.
- According to the comparison between ideal resistor, real resistor (with extracted parasitics) and the model of polysilicon resistors “rpoly2”, which are situated in CADANCE can be said that the used “rpoly2” model has AC magnitude and phase, which coincides with the ideal one.
- Examined real polysilicon resistors “rpoly2” has magnitude and phase, which coincide with this of the ideal resistor in the frequency range from 1Hz to 10GHz.

6. REFERENCES

- [1] Hastings, A., *The Art of Analog Layout*, Prentice Hall, 2003, ISBN 0-13-087061-7.
- [2] Harame, D., A. Joseph, *The Emerging Role of SiGe BICMOS Technology in Wired and Wireless Communications*, Fourth IEEE International Caracas Conference on Devices, Circuits and Systems, Aruba, April 17-19, 2002.
- [3] Grebene, A., *Bipolar and MOS Analog Integrated Circuit Design*, John Wiley and Sons, 2nd edition, 2003, ISBN 0-471-08529-4.