MONOLITHIC SPIRAL INDUCTORS DESIGN FOR RF APPLICATIONS

B. Sc. Janeta Stefcheva Sevova, M. Sc. Diana Ivanova Pukneva, Assoc. Prof. Ph. D. Marin Hristov Hristov

ECAD Laboratory, Technical University of Sofia, 8 Kliment Ohsridski Str., 1797 Sofia, Bulgaria, Phone: (+3592)9653115, e-mail: jss@ecad.tu-sofia.bg, pukneva@ecad.tu-sofia.bg, mhristov@ecad.tu-sofia.bg,

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Inductors are designed on silicon (Si) substrate with inductance value from 1-10 nH and quality factor up to 10 for AMS 0.35mm BiCMOS technologies. A custom computer-aided-design program called ASITIC (Analysis and Simulation of Inductors and Transformers for Integrated Circuits) is used for design, analysis and optimization. Created in ASITIC structures are optimized and verified with simulations in Cadence.

1. INTRODUCTION

In the last few years the interest in the high frequency applications – circuitry and design increases. These circuits can be used in portative devices for wireless communications. The main idea is to implement all passive and active components used in a RF device on single chip. Passive components such as inductors and the transformers, implemented on a single chip are very important, because they are the heart of the transceiver.

Monolithic chip inductors are plate coils, made using low resistive layer. In order to reduce the capacitive coupling between the metal layer and the substrate the uppermost metal layer is used for the inductor. The exit from the inner coil end is made by transition to other metal layer (underpass). Cross section of square spiral inductor is shown in fig. 1. In fig. 2 are given its geometry parameters: outer diameter d_{out}, width of the metal strip w, space between neighbouring segments s and number of turns n. Metal M3 and M4 are the metal layers used for the inductor and Via3 is the contact via for transition.

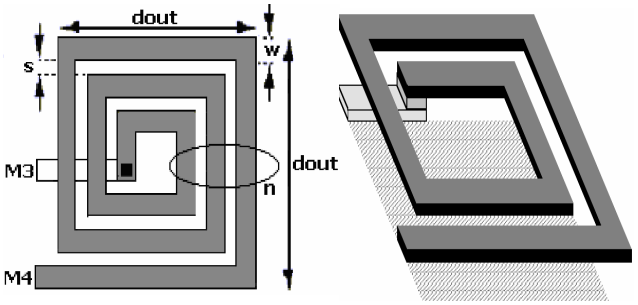

Fig.1 Cross section of spiral inductor

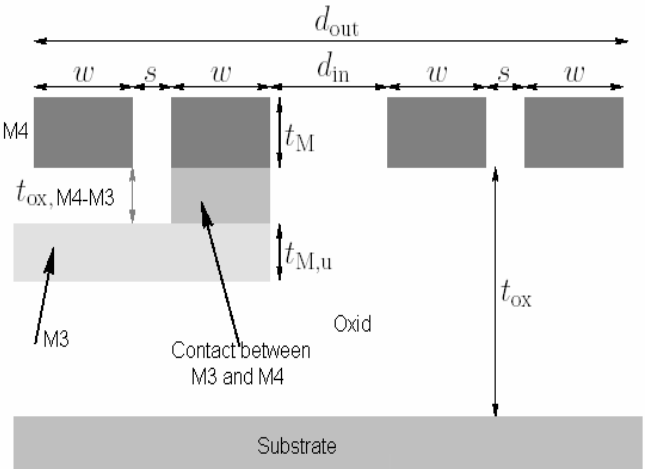

Fig. 2 Monolithic spiral inductor structure

2. DESIGN OF MONOLITHIC INDUCTORS

Two important groups of parameters have influence on the quality factor of the inductor: geometrical parameters and technological parameters. In the first group are the parameters, which can be changed from the designer as area and shape of the inductor, width of the metal strip and the space between neighbouring segments, and number of turns. In the second group can be included, substrate resistance, metal sheet resistance, and etc., which are specific for the technology and could not be changed.

At high frequencies inner coils has very big resistance, because of the eddy currents and as a result the quality factor decreases. So in the design are used inductors without inner coils (Hollow coil).

For the design of monolithic inductors is used the program called ASITIC (Analysis and Simulation of Inductors and Transformers for Integrated Circuits) and design rules for AMS BiCMOS SiGe 0.35 μm technology. The designed inductors are with outer diameter from 300 to 400 μm, metal strip width from 20 to 25 μm and space between neighbouring segments from 2 to 3 μm. Inductors are created using the uppermost fourth metal layer. Equal sizes are used to compare the results.

3. ANALYISIS OF MONOLITHIC INDUCTORS

In ASITIC electromagnetic analysis is used to investigate the monolithic inductors. They are presented with Pi – equivalent circuit (fig. 3).

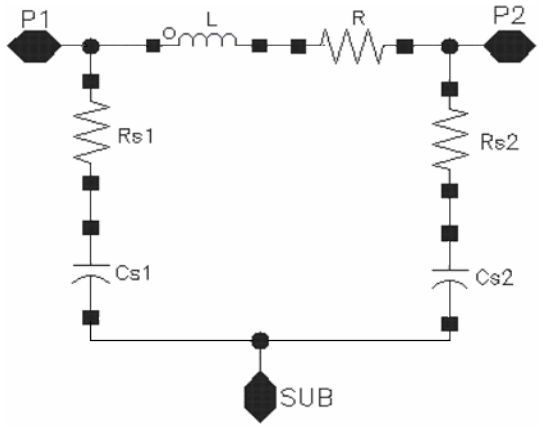

Fig. 3 Pi equivalent circuit of spiral inductor

Table 1 Model parameters of sq1 inductor

Name of the inductor	F GHz	Q_1 -	Q_2 -	Q_3 -	L nH	R Ω	C_{s1} fF	C_{s2} fF	R_{s1} Ω	R_{s2} Ω	f_{res} GHz
sq1	1	6.71	6.75	6.89	3.54	3.15	91	85.9	1.92k	2.45k	8.87
	2	10.10	10.32	11.02	3.51	3.69	50.7	42.9	1.17k	1.67k	11.94
	3	11.52	12.04	13.57	3.49	4.14	39.6	31.5	721	1.08k	13.54
	4	11.79	12.62	15.12	3.53	4.54	35.2	27.2	470	722	14.28
	5	11.25	12.36	15.79	3.58	4.94	33.2	25.2	324	506	91.81
	6	10.21	11.55	15.74	3.66	5.36	32.1	24.1	235	372	20.51
	7	8.72	10.19	14.72	3.74	6.11	31.4	23.4	178	283	17.11
	8	7.27	8.85	13.69	3.86	6.75	31.1	23	139	222	15.8
	9	5.76	7.42	12.4	4.01	7.49	30.9	22.8	111	179	15.03
	10	4.24	5.96	10.88	4.2	8.43	30.8	22.7	91.2	147	14.45

The model parameters of one of the spiral inductors sq1 are shown in Table 1. The values are for the frequency range from 1 to 10 GHz. Some simulation results from the analysis of the inductors are given in Table 2.

Table 2 Analysis results of spiral inductors

№	Naeme of the inductor	d_{out}, μm	w μm	s μm	N	$f(Q_{max})$ GHz	Q_1 -	Q_2 -	Q_3 -	L nH
1	sq1	300	20	2	3	5	10.10	10.32	11.02	3.51
2	sq2	300	25	2	3	6	9.68	9.91	10.5	2.87
3	sq3	300	25	2	4	5	8.18	8.45	8.89	3.49
4	sq4	300	25	2	5	5	6.37	6.55	6.83	3.59
5	sq5	300	25	3	4	5	8.28	8.56	8.99	3.35
6	sq6	300	25	3	5	6	6.35	6.53	6.84	3.36
7	sq7	350	20	2	3	4	10.44	10.70	11.97	4.65
8	sq8	350	25	2	3	4	10.46	10.80	11.85	3.91
9	sq9	350	25	2	4	4	8.80	9.27	10.45	5.07
10	sq10	350	25	2	5	3	7.35	7.84	8.77	5.68
11	sq11	400	20	2	3	3	10.08	10.52	12.38	5.88
12	sq12	400	25	2	3	3	10.30	10.85	12.49	5.05
13	sq13	400	25	2	4	2	8.57	9.30	11.00	6.85
14	sq14	400	25	2	5	2	7.17	7.97	9.44	8.12
15	sq15	400	25	3	4	3	8.72	9.50	11.18	6.64
16	sq16	400	25	3	5	2	7.37	8.23	9.69	7.78

4. INDUCTOR VERIFICATIONS IN CADENCE

The designed inductors in ASITIC can be transferred in CADENCE as CIF (Caltech Interchange Format) file, to see and verify their geometry. The inductors performance is optimized with the CAD system CADENCE. Guard rings and shields are added respectively for better isolation from adjacent elements and to reduce the eddy currents.

Optimized topology of an inductor in CADENCE is shown in fig. 4.

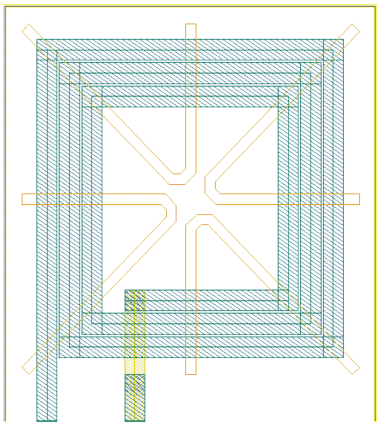

Fig. 4 Topology of optimized inductor in CADENCE

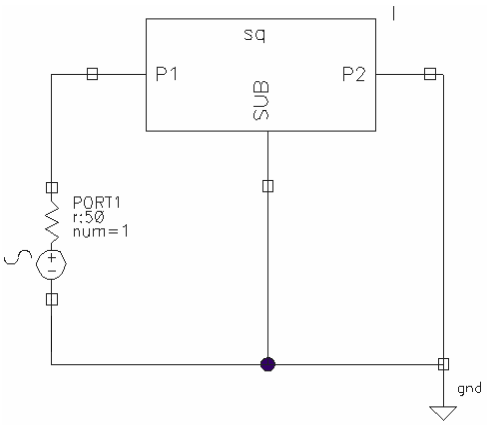

Fig. 5 Q factor simulation circuit

5. COMPARISON OF ASITIC AND CADENCE SIMULATION RESULTS

In order to verify the results, received in ASITIC, the quality factor Q of the inductors is investigated in CADENCE using the circuit presented in fig. 5. In

CADENCE are utilized the models of the inductors for 2 GHz, because the pi – equivalent circuit model is frequency dependent. The values of the parameters, necessary for CADENCE model are calculated in ASITIC. Quality factor of the inductors is simulated in ASITIC and CADENCE. Thus, comparison can be made. The error in the selected frequency range is from 0 to 5%. The results are listed in Table 3.

Table 3. Quality factors investigated in ASITIC and CADENCE

№	Name of the inductor	Q_1 , -	$Q_{ИКМ}$, -
1	Sq1	10.1	10.11
2	Sq2	9.68	9.692
3	Sq3	8.18	8.199
4	Sq4	6.37	6.338
5	Sq5	8.28	8.311
6	Sq6	6.35	6.358
7	Sq7	10.44	10.46
8	Sq8	10.46	10.47
9	Sq9	8.8	8.814
10	Sq10	7.35	7.354
11	Sq11	10.08	10.07
12	Sq12	10.3	10.31
13	Sq13	8.57	8.576
14	Sq14	7.17	7.161
15	Sq15	8.72	8.7
16	Sq16	7.37	7.37

The used in CADENCE model of the designed inductors is for specific frequency (2GHz) and a narrow band around it. But the simulations are performed for frequency range from 1 to 10 GHz. Thus, the deviation from the real value is calculated for the quality factor Q_1, inductance L and serial resistance R_s. Results received from these measurements and absolute errors are given in the tables below.

The measurements for the quality factor Q are shown in fig. 6.1 for ASITIC, in fig. 6.2 for CADENCE and in Table 4 - the error between CADENSE and ASITIC for Q.

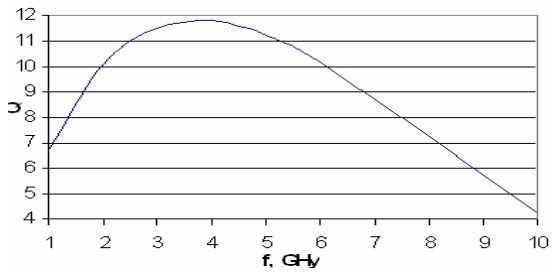

Fig. 6.1 Q of sq1 inAsitic

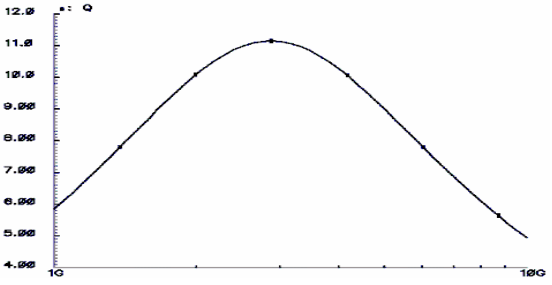

Fig. 6.2 Q of sq1 in Cadence

Table 4 Error between Asitic and Cadence for Q

f,GHz	1	2	3	4	5	6	7	8	9	10
δ , %	12.67	0	3.39	12.89	20	23.21	20.99	16.09	5.03	-16.7

The measurements for the inductance L are shown in fig. 7.1 for ASITIC, in fig. 7.2 for CADENCE and in Table 5 - the error between CADENSE and ASITIC for L.

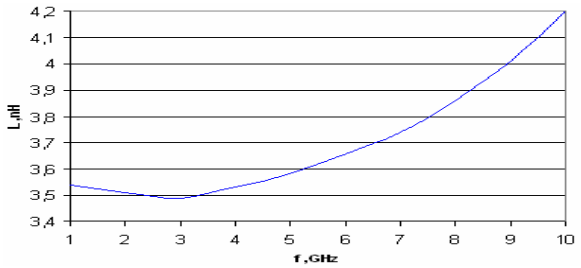

Fig. 7.1 L of sq1 in Asitic

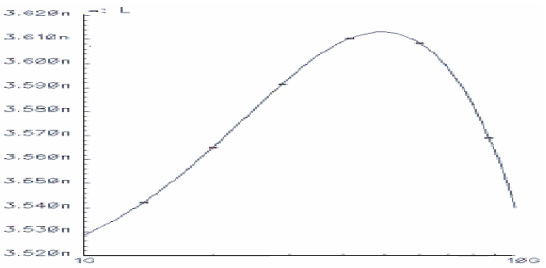

Fig. 7.2 L of sq1 in Cadence

Table 5 Error between Asitic and Cadence for L

f,GHz	1	2	3	4	5	6	7	8	9	10
δ , %	0.28	-1.71	-2.87	-2.27	-0.84	1.37	3.7	7.25	11.22	15.71

The measurements for the serial inductance R are shown in fig. 8.1 for ASITIC, for CADENCE in fig. 8.2 and in Table 6 - the error between CADENSE and ASITIC for R.

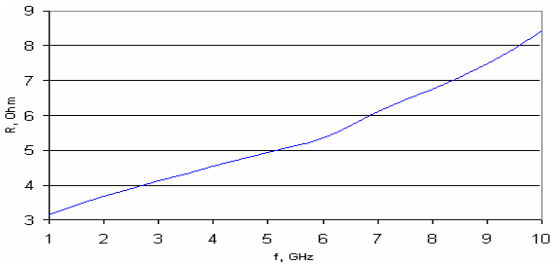

Fig. 8.1 R of sq1 in Asitic

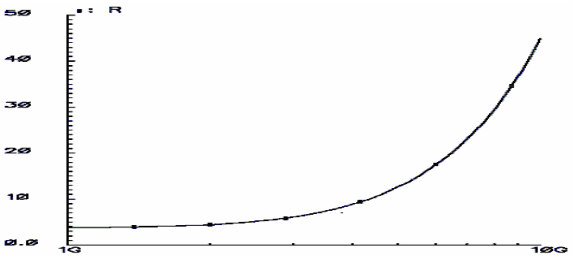

Fig. 8.2 R of sq1 in Cadence

Table 6 Error between Asitic and Cadence for R

f,GHz	1	2	3	4	5	6	7	8	9	10
δ , %	-20.3	-20.3	-47.1	-94.5	-155	-224	-277	-338	-392	-434

Results for the absolute error are most accurate for frequency 2GHz and with increasing the frequency, the error is increased.

6. CONCLUSIONS

The following conclusions can be made from the research made CADENCE and ASITIC:

- The quality factor of the integrate inductors created using 0.35 BiCMOS SiGe technology are up to 10. After the optimization the quality factor has is a little bit higher.
- The inductor model designed in ASITIC is frequency depended and gives accurate values for the inductance only for the given frequency and the narrow band around it. Thus, multiple simulations must be done. Simulations are performed for 1 to 10 GHz with 1 GHz step. The results taken from ASITIC are considered as a reference for the simulations in CADENCE.

- Inductor model implemented in CADENCE is for 2 GHz frequency. After the simulations in the frequency range from 1 to 10 GHz, the error introduced using narrow-band frequency depended model is calculated for the quality factor, the inductance and the serial resistance value.

7. OPTIMIZED INDUCTORS AND THEIR QUALITY FACTORS

In fig. 9.1, fig. 10.1, fig. 11.1, are shown some of the optimized inductors in CADENCE and in fig. 9.2, fig. 10.2, fig. 11.2 are shown their quality factors Q.

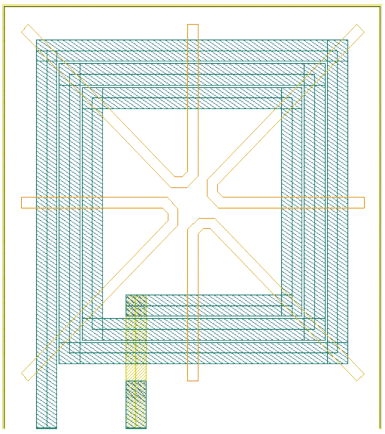

Fig. 9.1 Topology of sq1

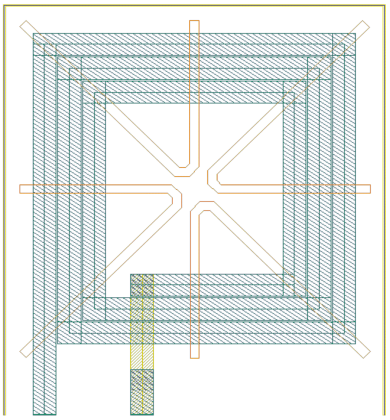

Fig. 10.1 Topology of sq8

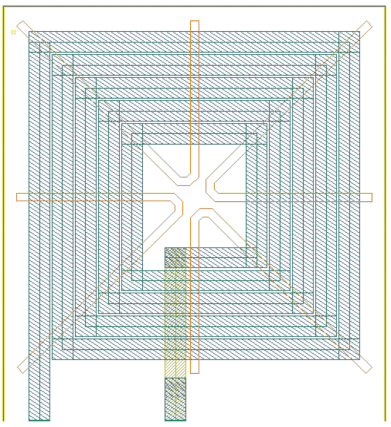

Fig. 11.1 Topology of sq16

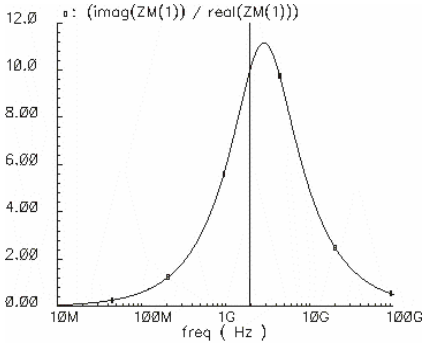

Fig. 9.2 Q of sq1

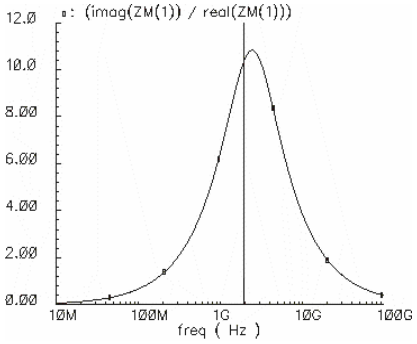

Fig. 10.2 Q of sq8

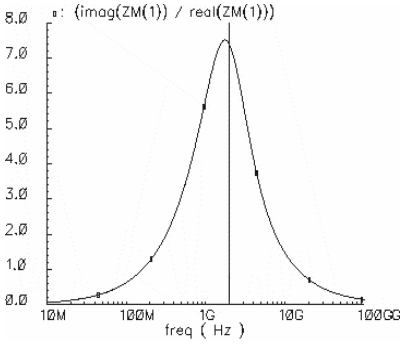

Fig. 11.2 Q of sq16

8. REFERENCES

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