AN ADVERTICING MODUL, DEVELOPED ON THE BASE OF A CPLD PROGRAMABLE DEVICE

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A design of an advertising module, developed on the base of a chosen typical contemporary structure of a reprogrammable CPLD device from the series XC9500, a produce of the firm Xilinx, is presented in the paper. The choice had been made according to the following circumstances: easy accessibility of the devices from this type, low cost, a comfortable programmer assurance for programming and reprogramming, offered freely by the Internet from the firm developer. For the development of the project an integrated system WebPack (ver 6.2) of the firm Xilinx is used. For the realization of the idea a VHDL description of the block scheme of the designed advertising module is used. The CPLD device is configured in laboratory conditions “in system programmable”. The programming of the scheme is being made according to the standard IEEE 1149.1 JTAG, by means of a specialized programmer CPLD XC95XL Design Board, connected through JTAG (Joint Test Action Group) cable for communication to the parallel port of the personal computer.

1. INTRODUCTION

An advertisement is necessary for the success of every human activity. The first of all, the advertisement means information. Every announcement, made in connection with a trade, handcraft, occupation or training with the aim of stimulatig the realization of commodities or services, is an advertisement. But it can provoke a bigger effect with its sudden appearance, rather than with its constant disposition in a determined place. Unlike the traditional advertisement (in the newspapers, on the radio, on the television), the advertisement can become constantly accessible if it is developed separately in some connection and if it is put on the specified place. With the aim to become more attractive, the advertisement should be dynamical and in combination with different light effects. For this and other purposes, an advertisement module is developed on the base of a CPLD programmable device of the firm Xilinx. In this work we suggest a new approach in the technology of the designing of digital devices. Now the products of the firm Xilinx are easy accesible and at comparatively low cost. Except this the same firm suggest also an integrated system WebPack for automated designing and programming.

2. IDENTITY OF THE SUGGESTED SOLLUTION

An advertising module, designed according to the block scheme, shown on the figure 1, is suggested. The main blocks in that scheme are: *Generator* – for generating signals with a rectangular shape and determined frequency; *Start/Stop* *block* – in dependence of the output condition of this block impulses enter or not to the input of the *Divider of frequencies*, the frequency of which is divided with predetermined coefficient of division; *Scheme of concurrence* – for harmonizing the common functioning of the generator and the start/stop block; *Divider of frequencies* – at the outputs of which the signals with determined low frequencies are formed; *Shifting register* – the assigned from the *Block for choice and entry of effects* "program" determines the way of the moving the information in the shifting register; *Light-emitting diode output circuit* – the every of the outputs of the shifting register command an separate circuit for obtaining light effects; *Supply block* – providing all necessary voltages for the module.

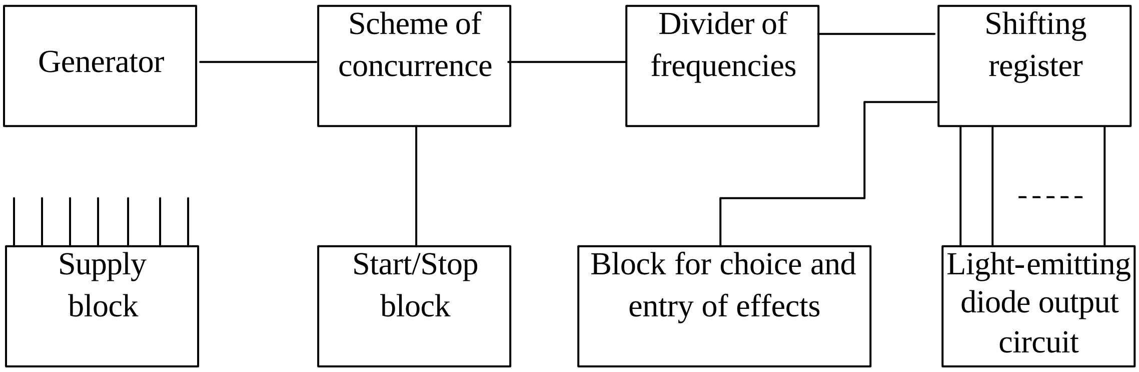


Fig.1. Block scheme of the designed advertisement module

For the creation of the advertising module we used a highly productive device of the type CPLD of the firm Xilinx from the family XC9500 and more concretely the integrated circuit XC9572XL. This choice is based on the advantages, such as easy designing and revision of the project, a possibility for multiple reprogramming of the device without a necessity to switch off the supplying voltage, energy independence during work in respect of preserving the project, a possibility to work with TTL and CMOS logical levels at supplying with 3.3V and 5V and low cost [1, 2].

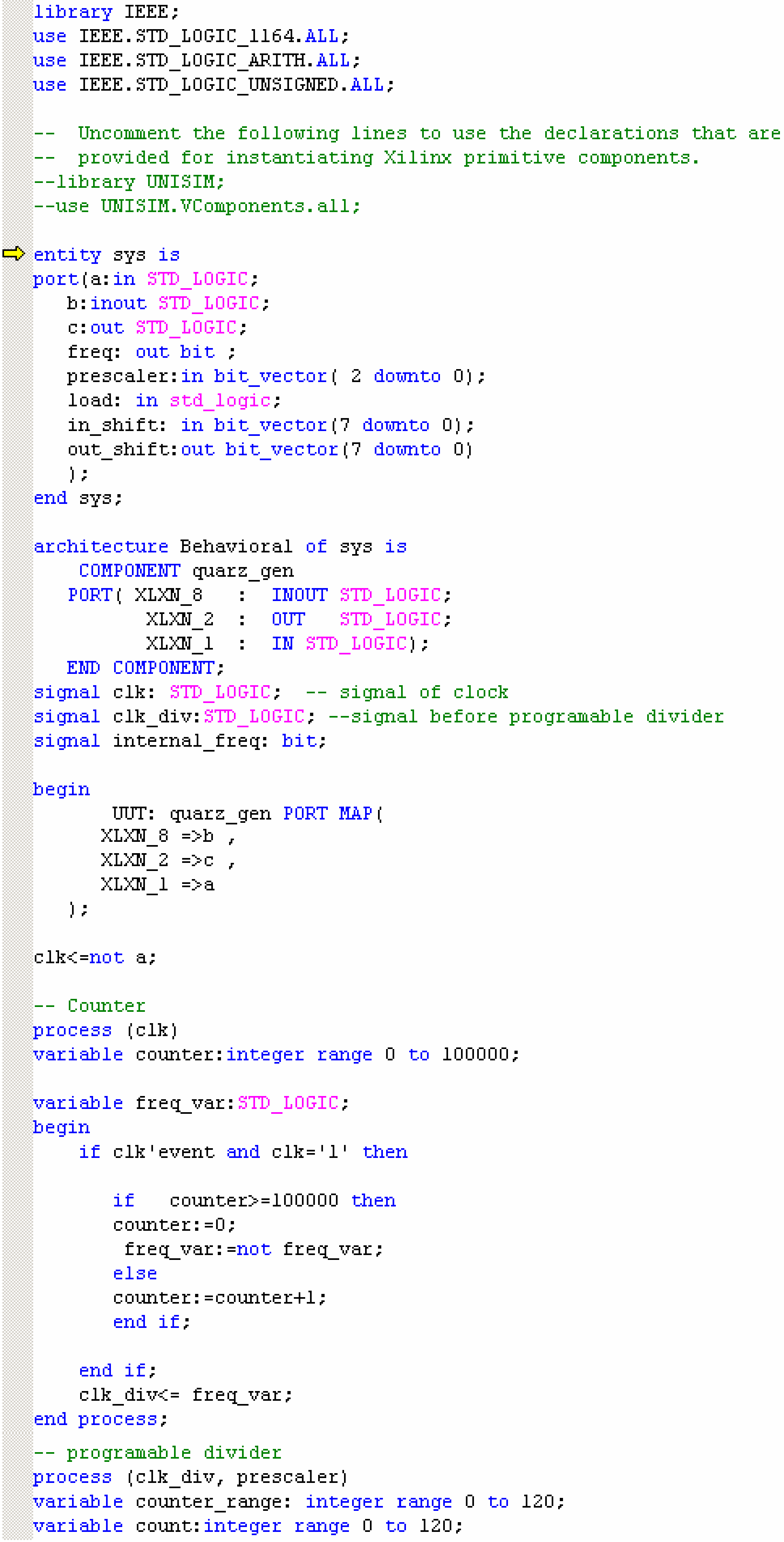
The design of the advertisement module can be performed with the help of the graph redactor Schematic Editor from the design medium WebPack. In this case one has to dispose with a preliminary designed and synthesized by the classical method scheme. For the introduction of the scheme, the attachment libraries of the graph redactor are used. For the creation of the scheme when a new project is prepared one starts the Project Navigator and from the window Top-Level Module Type selects the type of the module (from the language of a hardwere description HDL). One choose the programable device, the type of the corps and its parameters for funtion are determined (the adjustments of the ship are made). From the next window Create a New Source the type of the module Schematic is indicaed. The next step is starting the graph redactor, with which the scheme will be introduced, as the name of the fyle is given preliminarily. After its drowing, the scheme is saved. A programme for logical synthesis is used for transforming the graphically introduced scheme in the netlist, with the help of which the different logical elements and the connections between them are described. It follows framing, Implement Design of the project to the chosene CPLD device and simulating the work of the module to receive data for its work capabilities.

By means of simulation with ModelSim simulator one can receive the time diagrames of the sintezied advertisment module. From the analisis of the time diagrames a conclusion can be made, that the designed module functions correctly and in accordance with the assignment. Under this conition one can proceed to the next step, which is the programming of the device itself. It is performed with the help of XC9500XL Development Kit, for example, that of the firm Memec.

This method of approach with CPLD logic beginning with an introduction of the description of the logical scheme with the help of the graph redactor Schematic Editor (it begins with the creation of the scheme) is preferable, when the designer is not acquainted with the languages of high level for hardware description and when the projects are comparatively small. It is even better, when prepared modules of attached libraries are being used. If an error occurs during the synthesis and drawing the scheme, it is not possible to check the syntax of the generated from the product VHDL description (which remains hidden for the designer). That's why in some cases (when the designer don't dispose with ready digital logic scheme), the synthesis of the scheme is done with an application of classical methods, as these advantages are being taken into account.

The presented approach is not suitable for more complicated projects. That's why for the design of the advertisement module a language VHDL is used as a language for description of the apparatus means of the scheme. One begins with the creation of VHDL description of the preliminary sugested block scheme, shown on the fig.1. For this purpose the Project Navigator is started. From File\New Project a name is given to the project (Project Name: sys). From the window Top-Level Module Type the type of the module is idicated (trough the language of hardware description HDL). One chooses the programable device, the type of the corps and its parameters for funtioning are determined (the adjustments of the ship, in the case XC9572XL, are made). From the next window Create a New Source the type of the of the module is indicated (in the case VHDL Module). The full VHDL descrition of the components of the digital scheme is introduced. In the architecture part of every one of the components a mark is held, which assigns the induvidual models (conditions) of the outputs in dependence of the number of the conditions at the inputs. After the creation of the VHDL descriptions of the separate components of the systhem, a check for syntax errors is performed. The fragments of the programme for description of the designed advertisment module are created according to the chousen block scheme and are presented on the fig.2. [3-6].

The operator *entity* consists of descriptions of the input and the output interface of the project, since every system (scheme) has inputs and outputs. As it is seen, the name of the module and the characteristics of its inputs and outputs are given in the description of the interface. In the case bit vektor (2 downto 0), bit vektor (7 downto 0) and bit vector (7 downto 0) are bit vectors with a length 3, 8 and 8 bits correspondingly.



```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

--  Uncomment the following lines to use the declarations that are
--  provided for instantiating Xilinx primitive components.
--library UNISIM;
--use UNISIM.VComponents.all;

entity sys is
port(a:in STD_LOGIC;
   b:inout STD_LOGIC;
   c:out STD_LOGIC;
   freq: out bit ;
   prescaler:in bit_vector( 2 downto 0);
   load: in std_logic;
   in_shift: in bit_vector(7 downto 0);
   out_shift:out bit_vector(7 downto 0)
   );
end sys;

architecture Behavioral of sys is
    COMPONENT quarz_gen
   PORT( XLXN_8   :  INOUT STD_LOGIC;
          XLXN_2  :  OUT   STD_LOGIC;
          XLXN_1  :  IN STD_LOGIC);
   END COMPONENT;
signal clk: STD_LOGIC;  -- signal of clock
signal clk_div:STD_LOGIC; --signal before programable divider
signal internal_freq: bit;

begin
       UUT: quarz_gen PORT MAP(
      XLXN_8 =>b ,
      XLXN_2 =>c ,
      XLXN_1 =>a
   );

clk<=not a;

-- Counter
process (clk)
variable counter:integer range 0 to 100000;

variable freq_var:STD_LOGIC;
begin
    if clk'event and clk='1' then

       if   counter>=100000 then
       counter:=0;
        freq_var:=not freq_var;
       else
       counter:=counter+1;
       end if;

    end if;
    clk_div<= freq_var;
end process;
-- programable divider
process (clk_div, prescaler)
variable counter_range: integer range 0 to 120;
variable count:integer range 0 to 120;
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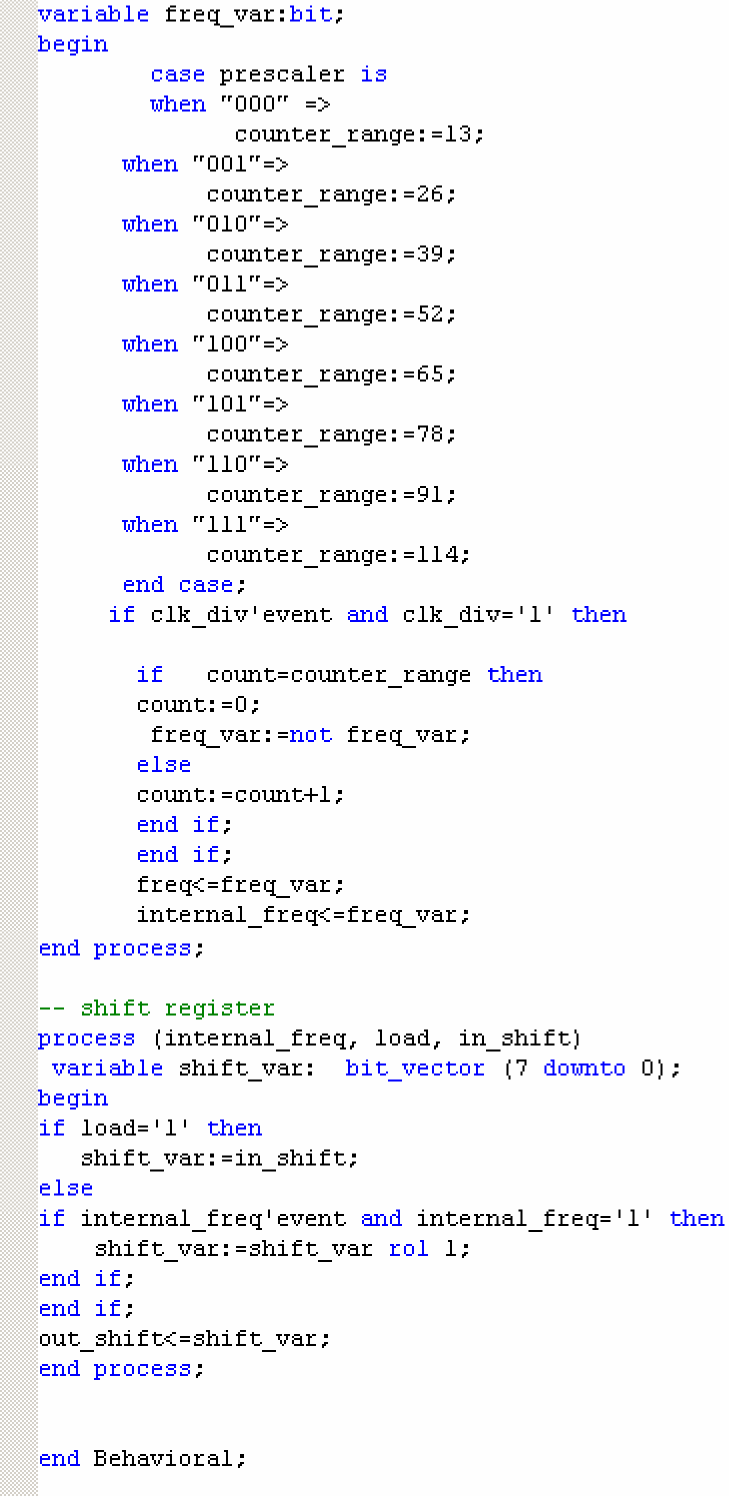


```
variable freq_var:bit;
begin
        case prescaler is
        when "000" =>
              counter_range:=13;
      when "001"=>
            counter_range:=26;
      when "010"=>
            counter_range:=39;
      when "011"=>
            counter_range:=52;
      when "100"=>
            counter_range:=65;
      when "101"=>
            counter_range:=78;
      when "110"=>
            counter_range:=91;
      when "111"=>
            counter_range:=114;
      end case;
     if clk_div'event and clk_div='1' then

       if   count=counter_range then
       count:=0;
        freq_var:=not freq_var;
       else
       count:=count+1;
       end if;
       end if;
       freq<=freq_var;
       internal_freq<=freq_var;
end process;

-- shift register
process (internal_freq, load, in_shift)
 variable shift_var:  bit_vector (7 downto 0);
begin
if load='1' then
   shift_var:=in_shift;
else
if internal_freq'event and internal_freq='1' then
    shift_var:=shift_var rol 1;
end if;
end if;
out_shift<=shift_var;
end process;


end Behavioral;
```

Fig. 2. VHDL description of the advertising module

In accordance with the made description of the interface of the project, the block scheme, shown on the fig. 3, is generated. After the creation of the module one passes over to the introduction of its behavior description. The components of the modules are presented in the following consistence: *Counter*, *Programmable divider* and *Shift register*. Preliminary prepared modules, such as the module *Generator*, are being used.

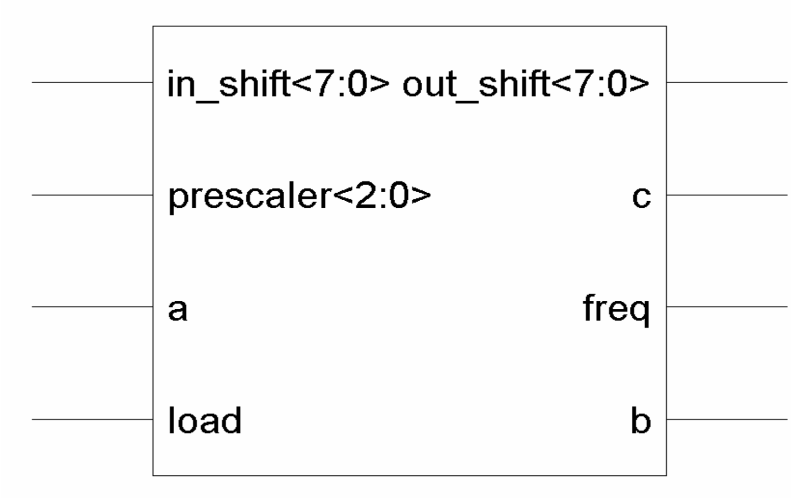
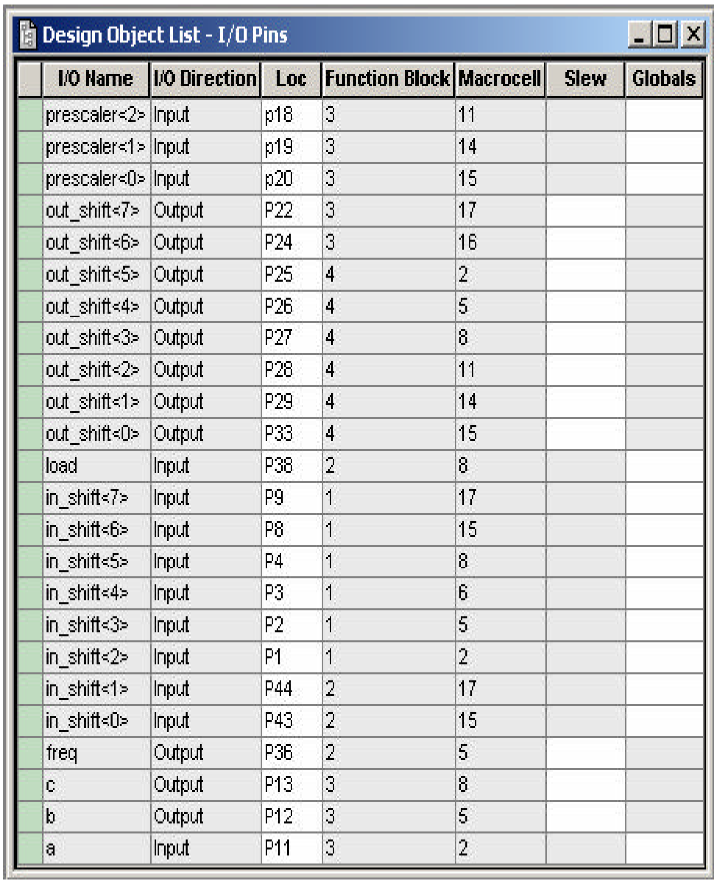


Fig. 3. Bock scheme of the advertising module, prepared after VHDL description of the connections between different components of the digital system

On the figure 4 one can see the terminals of the integrated circuit and their appointments. With the help of 3 micro switchers on pins P18, P19 and P20 one assigns 8 different work frequencies. On pins P22, P24, P25, P26, P27, P28, P29 and P33 the effects in shiftreg are assigned.

3. CONCLUSION

An advertising module is designed, which with the shown possibility for different light effects allows representation of different activities and products in dynamical regime. The advertising module, as model can be used also for the purposes of the education during the study and implementation of the programmable logic. It is realized on the base of the chosen typical contemporary structure of the reprogrammable CPLD device from the series XC9500, produced from the firm Xilinx. The whole module, or parts of it, can be used also during the development of new projects with CPLD logic.



	I/O Name	I/O Direction	Loc	Function Block	Macrocell	Slew	Globals
	prescaler<2>	Input	p18	3	11		
	prescaler<1>	Input	p19	3	14		
	prescaler<0>	Input	p20	3	15		
	out_shift<7>	Output	P22	3	17		
	out_shift<6>	Output	P24	3	16		
	out_shift<5>	Output	P25	4	2		
	out_shift<4>	Output	P26	4	5		
	out_shift<3>	Output	P27	4	8		
	out_shift<2>	Output	P28	4	11		
	out_shift<1>	Output	P29	4	14		
	out_shift<0>	Output	P33	4	15		
	load	Input	P38	2	8		
	in_shift<7>	Input	P9	1	17		
	in_shift<6>	Input	P8	1	15		
	in_shift<5>	Input	P4	1	8		
	in_shift<4>	Input	P3	1	6		
	in_shift<3>	Input	P2	1	5		
	in_shift<2>	Input	P1	1	2		
	in_shift<1>	Input	P44	2	17		
	in_shift<0>	Input	P43	2	15		
	freq	Output	P36	2	5		
	c	Output	P13	3	8		
	b	Output	P12	3	5		
	a	Input	P11	3	2		

Fig. 4. List with the outputs of the used CPLD device and their appointment

4. REFERENCES

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