DIGITAL CONTROLLER FOR SYNCRONOUS BUCK-BOOST CONVERTER

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Keywords: Digital controller, VHDL, Programmable Logic, Li-ion battery.

The proposed controller IC is digital and implemented in Xilinx CoolRunner II CPLD. It is designed to control a synchronous buck-boost converter. The input voltage can be lower, equal, or higher than the output voltage. This is significant advantage over the available controller ICs. In the proposed implementation, the input voltage can vary between 3V to 9V DC, the output voltage is 4,2V per cell at 300mA. The battery charge current and voltage are monitored through an external IC and internal CPLD Schmitt triggers. The controller architecture is custom and specially designed for this implementation. The digital controller model is developed with VHDL, using "top-down" design methodology. The verification is made with test vectors generated in VHDL test bench module.

1. INTRODUCTION

The digital controllers have many advantages over their analog counterparts such as ease of design, flexibility, optimization, and improved system reliability. In addition, digital offers an overall more elegant solution to many of today's demanding power requirements. Fundamentally, digital architectures differ from analog in the fact that digital controllers use A/D converters or special data acquisition circuits to digitize current and voltage information. The compensation and regulation is done by implementing different design techniques. The digital controller offers the ability to add, eliminate, or change any parameter in the system in order to meet new requirements, or to optimize and calibrate the system. Systems based on digital controllers require fewer components, which decreases the failure possibilities.

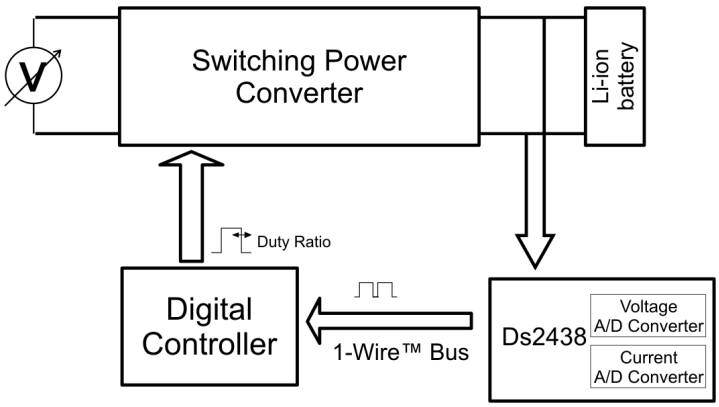

Figure 1. Li-ion battery charging system

This paper addresses the behavioral design and implementation of a digital PWM controller with a complex programmable logic device (CPLD). The considered operating environment of the controller is shown on fig.1. It consists of, Switching Power Converter, load – in this case is a single cell Li-ion battery, feedback circuit – DS2438. The controller drives the switching

power transistors of the converter. The communication with the battery monitor IC is implemented with 1-wire protocol.

2. DIGITAL CONTROLLER BLOCK DIAGRAM

2.1 Main interface signals

The main input/output signals and their function are presented in table 1.

Table 1. Digital Controller I/O Ports

Signal	Direction	Function
Clk_Sys	Input	Global system clock
Rst	Input	Global system initialization signal
One_wire	Input	Feedback signal from DS2438
Current_Level	Output	End of charge flag
St_Up1	Output	Driver signal for boost power transistor 1
St_Up2	Output	Driver signal for boost power transistor 2
St_Down1	Output	Driver signal for buck power transistor 1
St_Down2	Output	Driver signal for buck power transistor 2

2.2 Main blocks

The design of the digital controller is made with high-level hardware description language – VHDL. It can be used along with the top-down design methodology. The blocks which comprise the system are specified by their function and behavior as well as I/O interface. The block diagram is presented on figure 2.

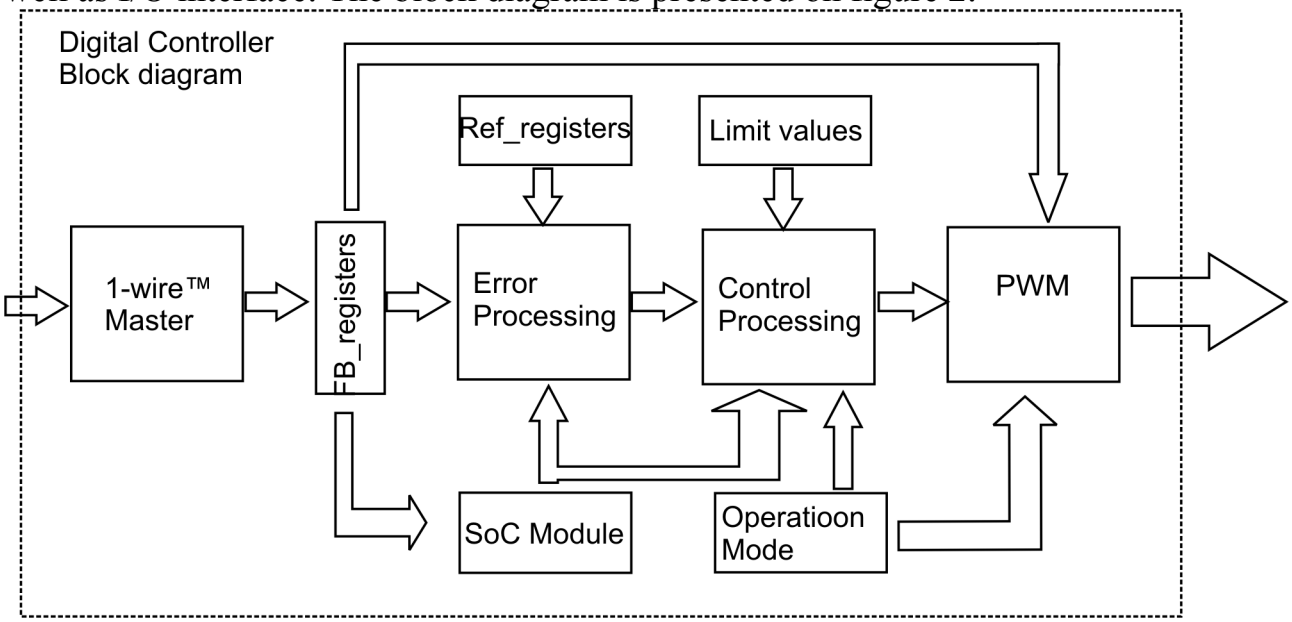

Figure 2. Block Diagram

- **1-wire master.**

The 1-wire™ master module has the task to communicate with the DS2438 smart battery monitor through a 1-wire™ serial interface. The module is master in the 1-wire network, and it sends commands to the slave device implemented in the battery

sensor. The communication is based on exact time intervals for sending information on the 1-witre bus. The master commands are synchronized with the current state of charge (SoC) status.

- **FB_registers**

This block is a simple buffer which holds the extracted values of the voltage and current values in 8-bit registers. The register values determine the state of charge status and are used by the PWM module to determine the end of charge status.

- **Ref_registers**

The reference values for the battery charge voltage and current are stored in the **ref_registers** block. These values represent the desired output voltage – 4,2V for a single cell li-ion battery, and the desired charge current of 300mA. The exact values are obtained by the transfer function of the DS2438 voltage and current ADC.

- **Error computation**

This module receives the information from the feedback registers block (**FB_registers**), the reference registers block (**Ref_registers**). These values are processed and the error value is computed.

$$\text{Error} = \text{ref\_register} - \text{fb\_register} \quad (1)$$

The format of the error value is 8-bit signed binary number. The MSB is the sign. A flag shows the sign of the result.

A flag from the state of charge (**SoC**) module indicates the charge status. With this information the module determines which reference register to use – current or voltage.

- **State of charge (SoC)**

The module uses the information from the feedback registers and determines the controlled parameter – charge current or charge voltage. It toggles a flag to indicate the state in which the charge process is.

- **Limit values**

This module stores the limit values of the duty cycle for every one of the working modes and in every state of charge. These values are determined by practical simulation of a custom switch-mode power synchronous buck-boost converter. They can be changed for any application.

- **Operation Mode**

This module operates with the implemented Schmitt triggers in the Xilinx CoolRunner II™ CPLD. They are programmed to indicate the levels of the input voltage which determine the operation – buck converter, boost – converter or mixed buck-boost converter The mode of operation is a two bit register.

- **Control Processing**

The block has the task to compute the new value of the duty cycle of the working frequency.

The input data to this module is: the error value and its sign. The SoC flag, the operating mode status, the limit values. The operations which are performed are identical for the charge voltage control, and the charge current control. The only

differences are the values of the limit values for voltage and current. The controlled parameter is determined by the state of charge flag.

The error signal is used to determine the new value of the duty cycle register. With every rising edge of the system clock the new duty cycle register is evaluated. According to the sign flag the value of the reference register is incremented or decremented with the value of the error. If the value tries to go up or down the limit values the output registers are set to the value in **Limit values** block.

- **PWM Module**

The module drives the switch transistors of the power converter. The modulation is done by comparing the value of the input reference register with the value of a free running timer. When the values are equal the output pins toggle and the PWM is achieved. To verify the PWM module, a simulation was run. The achieved results are shown on figure 3.

The output signals drive the synchronous MOS switches. The operation mode register is used to determine the working driver signals.

The module toggles a flag which detects the end of charge if the value of the current feedback register goes below a certain value.

3. SIMULATION SYNTHESIS AND IMPLEMNTATION

The presented module was tested by applying test vectors using ModelTech ModelSim™ simulator.

Functional and post-fit simulations were run to verify the design. The former shows system's behavior in various working conditions and the latter determines calculated internal delays in device's modules. Particular results are shown in figure 4.

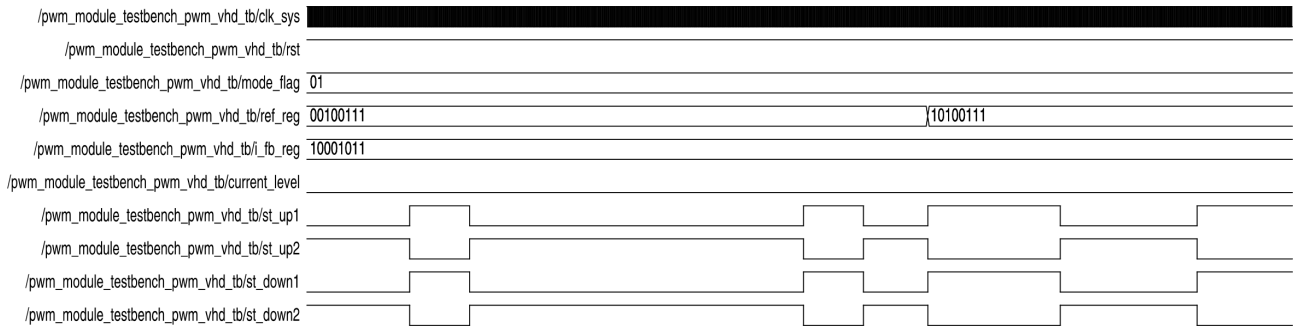

Figure 3. PWM module simulation waveforms.

PWM module simulation is shown on figure 3. It can be seen that the drive signals to the transistors are with modified duty cycle after the reference register is modified.

The control processing block is simulated behaviorally and against the timing models of the CPLD. The results are shown on figure 4.

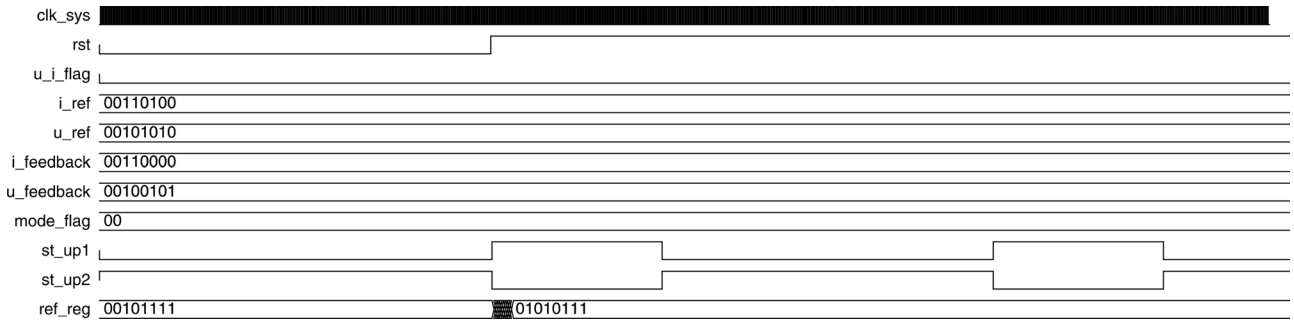

Figure 4. Digital Controller Simulation Waveforms. Reference register Computation.

The waveform represents the behavior of the control block, where the reference register for the PWM is calculated. The system clock is global to the whole system and all internal registers are synchronously working to it. The system is initialized externally with the signal **rst.** The active level of this signal is logical zero. When the signal is active the reference register takes the current value from the registers of the **limit value** module. The reference register value is computed and is used to obtain the new duty cycle of the working frequency. The signal st_up1 drives nMOS switch transistor and the signal st_up2 drives the pMOS. The two signals are inverted and form synchronous drive to the MOS transistor switches.

After computer simulations the design was implemented in a Xilinx CPLD (XC2C256-7TQ144). Implementation results are shown in Tables 1, 2 and 3.

Table 2. Overall CPLD Resource Utilization

Resources Summary				
Macrocells Used	Pterms Used	Registers Used	Pins Used	Function Block Inputs Used
120/256(47%)	562/896(63%)	31/256 (13%)	42/118 (36%)	332/640(52%)

Table 3. Pin IO Usage. Macrocell resources

PIN RESOURCES		
Signal Type	**Required**	**Mapped**
Input	35	35
Output	5	5
Bidirectional	0	0
GCK	1	1
GTS	0	0
GSR	1	1
MACROCELL RESOURCES		
Pin Type	**Used**	**Remaining**
I/O	35	73
GCK/IO	2	1
GTS/IO	4	0
GSR/IO	1	0

Table 4. Global resources

GLOBAL RESOURCES	
Total Macrocells Available	256
Registered Macrocells	31
Non-registered Macrocells driving I/O	1

The RTL schematic of the synthesized digital circuit is shown on figure 4.

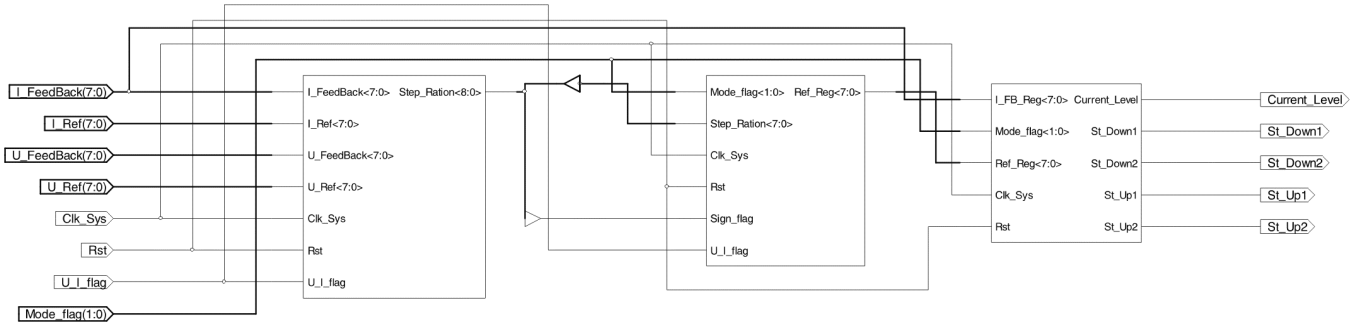

Figure 5.. RTL Schematic Of the synthesized Digitall Controller

4. CONCLUSION

Digital controllers are the building blocks of future innovation in power regulation. Digital offers system flexibility and optimization through a communication bus that just isn't achievable with today's analog controllers. Additionally, digital controllers offer improved time-to-market with ease of design and increased system reliability. The proposed digital controller has the ability to be reconfigurable. This advantage is achieved with the use of a Xilinx CPLD. The major advantage is the possibility to change the control algorithm even if the chip is already on the PCB. The communication protocols can be changed or replaced for specific application on the same chip. The clock frequency and the PWM frequency can be increased and the area and interconnect resources can be decreased. The use of top-down design methodology decreased the total design time. The high level hardware description language VHDL fully supports arithmetic and binary manipulations that are specific for such systems.

The future development of the portable systems will use less board space and fewer external components, which decreases the mean time before failure (MTBF) of the system.

5. REFERENCE

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