# TRANSFER THE PARAMETER BETWEEN ELEMENTS MODEL IN AC – DC DESIGN AREA FOR SIMULATION

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**Keywords:** parameters for synthesis and simulation, mixed simulation, models and interface, algorithm and characteristic.

*This paper is presented models of electronic elements witch work in AC – DC design area for synthesis and simulation. This paper discuss the questions of construct the interface between different models, characteristic this models of electronic elements or transfer the mixed parameter. Considering this qualities mixed presentation et transfer parameters electronic area obtain various manner. In publication prepositional variants of this interface trial run in mixed area. Area with mixed simulation ought to adapt models plus out signals or in signals. Adapt is correct mix of this signals. In similarity by prepositional interface are able making new objective models for specific case. Transfer the mixed parameter is dividing in four parts. Models are different type. Four groups is basic fundament and connections in these groups give cause for work in closed area. In this way reach universality allocation on post-processing. That will suffice for complex and very fine optimization.*

## 1. INTRODUCTION (WORK PROBLEM)

Many electronic schemas consist in analog and digital parts. Works with this scheme require AC-DC simulation. Analog parts and digital parts oneself different simulation. Analog simulator calculate tensions and currents, et digitals simulators – logical states ("1" , "O"). Algorithm of this work is very different. Analog simulators based in numerical method of differential equation and system equation.. In digitals simulators make used of specifically method for watch closely delay in logical scheme. This different point makes analog and digital simulations impossible with normal method. Coupling is difficult. In this situation designer must separated analog parts from digital parts et working from each parts particularly. Transfer the parameters is very difficulty if en elements exist opposite coupling between two parts. For that reason created mixed AC-DC simulators for big integrated elements. His combine in one various and speed of simulation, memory large and rout-trace in circuit design. Time of simulation is important parameter. Mixed simulation is tree pointing faster com normal (ordinary) simulation packet et its have little two point memory ram. In analysis work should one grand parts of time from correct lineal models for all Newton-Raphson descriptions. By good luck one large parts of elements is digital. Parts of digital elements is not normal activity end teen rate is have active tensions and currents from time interval simulations. This is fact make possible divide of parts or equations. Search sequence is [1] :

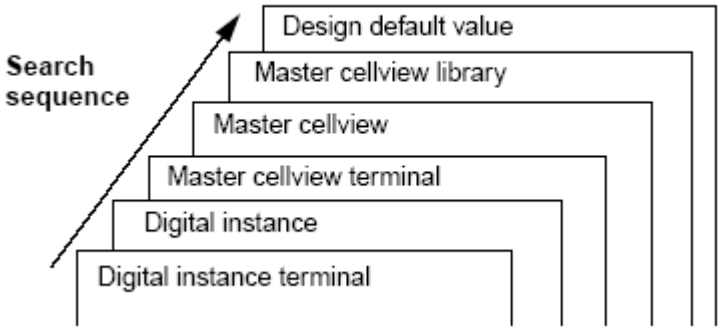



**Fig. 1.**

## 1.1. Interface of elements

Interface elements are generated automatically for input and output terminals of digital
components connected to interface nets. They do not appear on the schematic.
Interface elements consist:
_ Model the loading and driving impedance of digital instance terminals;
_ Convert voltages to logic levels, and vice versa;
_ Transport events between two simulators;
Each simulator uses interface elements to communicate its unique signal data type to other simulators. An interface element is a two-terminal device that connects two partitions and splits the original net, as shown in the following figure two. [1].

For each logical element have description of operators, and file consist function and operators, the one part of model. In-spice in line on description this method of work is placed in structure in figure 3. (for each part of element).

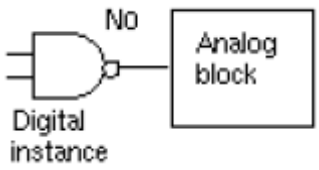



**Fig. 2.**

**Part of element a to D :**

```
++++++++++++++++++++++++++++++++++++++++
inline Spice Mos1_a2D
X&1,  &2,  C&1
.SUB CKT C&1, 1
da&1 1 0, a2d nestlev=1, dest=&1, vl=&3,
vh=&4, timeX=&5
VDD 4 0 5
R1 4 3 4K
Q1 2 3 1 0 TN1
R2 2 4 40K
R3 2 0 20K
. MODEL TN1 NPN …..
.ENDS C&1
```

**Fig. 3.**

Interface elements are not generated at interface nets that are global nets. Global nets are either global supply (static, constant) nets or global non-supply (dynamic, non-

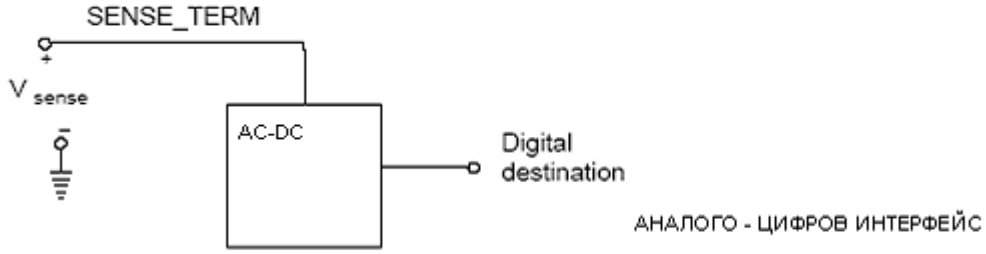
constant) nets. Powers and grounds are examples of supply nets. They do not change state and carry no events. A global clock is an example of a non-supply net. If a non-supply global net is an interface net, a warning is generated. A non-supply global net is either a design error or you must provide the appropriate analog or digital stimulus for the net.

**1.2. Mixed simulation. Transfer the parameters.**

Very important moment for mixed simulation the array is transfer the parameter between different elements of model (analog respectively digital). Exchange the information about parameters at mixed area is composite process alike important for work of array or important for correct simulation. Therefore et corrects reaction of models which get the parameters. This paper discuss the questions of construct the interface between different models, characteristic this models of electronic elements or transfer the mixed parameter. Considering this qualities mixed presentation et transfer parameters electronic area obtain various manner. In publication prepositional variants of this interface trial run in mixed area. In Spice program interface is default rational. On the figure [1], presented interface and status of point. This is function of voltage sense.

Analog-to-Digital AC-DC Models

The following figure shows the cdsSpice A2D interface primitive.




The following figure shows the digital destination as a function of voltage sensed.

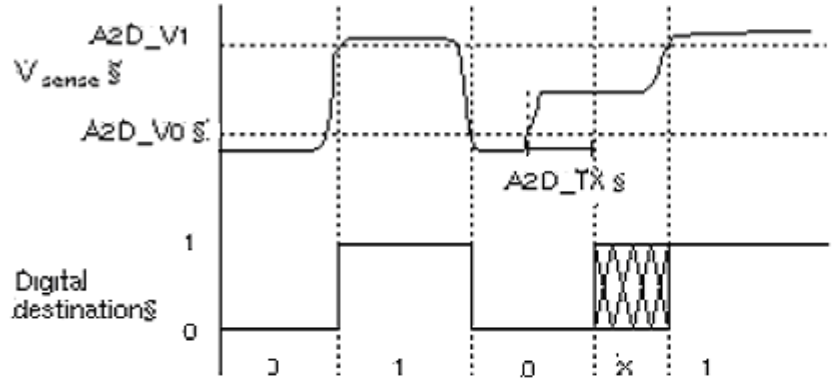



**Fig. 4.**

Interface of elements presented in diagram 4:

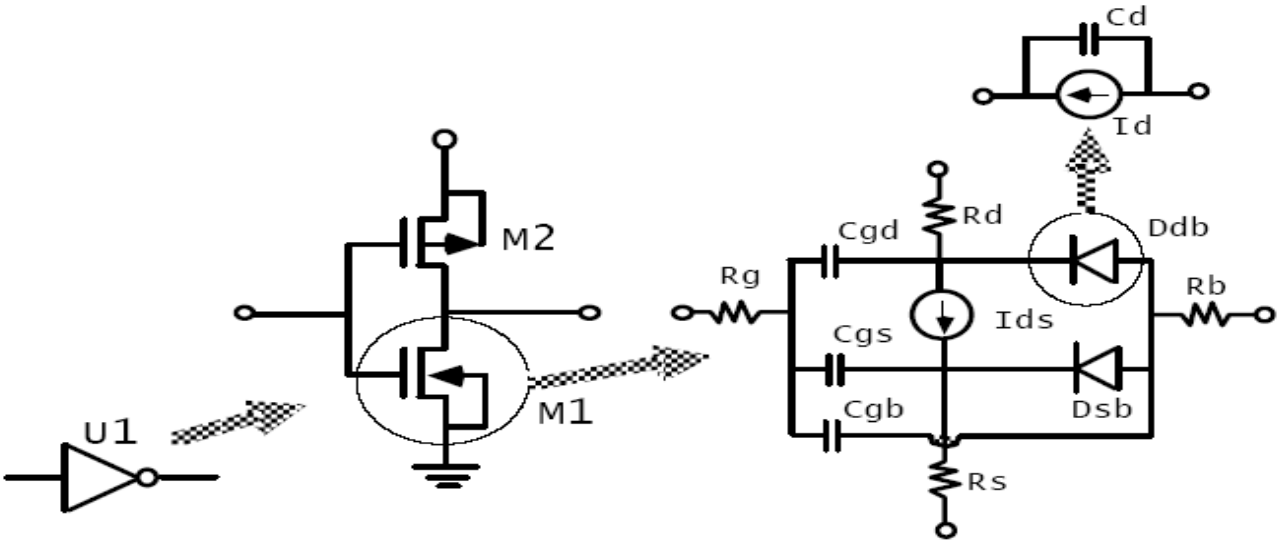
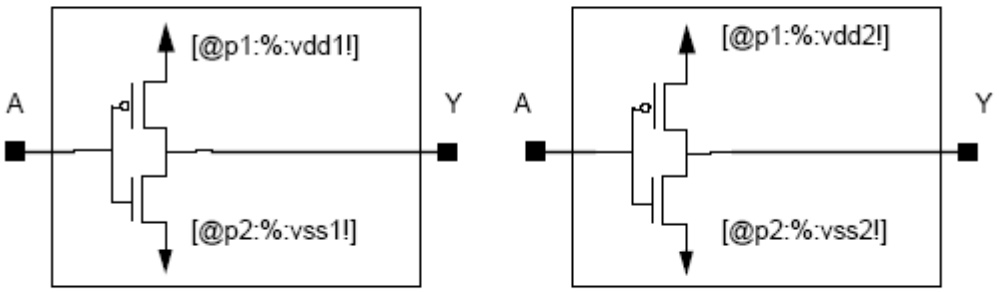



**Fig. 5.**

For approximation of element used SDF or Spice parameters.

| Properties from CDF | cdsSpice Properties |
|---|---|
| macro = MOS1_a2d | macro reference = MOS1_a2d.*S* |
| a2d_v0 = 1.5 | &3 = 1.5 |
| a2d_v1 = 3.5 | &4 = 3.5 |
| a2d_tx = 1m | &5 = 1m |

Below are examples of primitive cellviews with inherited connections. Cells A1 and A2 are analog. Cells D1 and D2 are digital. For illustration purposes, A1 and D1 have the same connectivity, and A2 and D2 have the same connectivity.




Analog cellview A1
Digital cellview D1

Analog cellview A2
Digital cellview D2

**Fig. 6.**

For description used function or procedure with mathematical formulation. These processes begin from each element of design end closed with equation formulation. Each procedure is only specifically, et his characteristic formula is virtual. Parameters accepted value from description of models et transfer this parameter whit program code. With this code realize port only for used model. R-port is idea Affrima used in [2], [3] et elaborate in this work. Program created used R-port from most for transferring of each parameter in model. In paper transfer only two parameter, level of digital signals and delay of this signal.

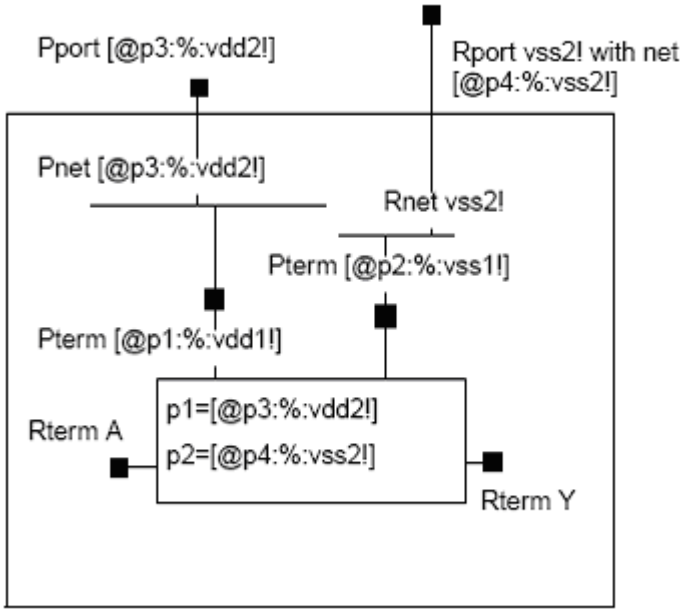



**Fig. 7.**

## 2. CONCLUSION:

1. Presented interface from transfer parameters from analog to digital part.
2. Used tree level status of logical elements, this "1", "0" and "x".
3. Make approach of interface (transistor, model, description, function). Fig. 5.
4. Used macro-model of Affrima [1].
5. In demo program used A1, A2, - AC element and this model and D1, D2 – DC element and his model. Fig. 6.
6. Interface created in R-port program for transfer the parameter. In case work with level and delay parameter [ 2 ].
7. Most of R-port presented in Fig.7.

## 3. REFERENCES

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