MIXED SIGNAL MULTI-LEVEL CIRCUIT SIMULATION

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Keywords: multi-level simulation, mixed simulation, models and interface, transfer the parameters.

This paper presented tree part of process design and simulation in array network. This is problems of design and including the part of elements et his parameters. Second moment is post-processing and algorithms of calculating and property work program and system. End finish problem of this process is structure of models end physical parameter of these models (dynamic and abstract). En literature terminology is using process of name mixed-signal, mixed-level, and multi-level (block, circuit, and device) This publication introduce case by way of example for mixed simulations in 4-bit ring counter et results is compare with 4-bit full ADDER (48 logic gates, 224 transistors)

1. INTRODUCTION

Every time slight error of heaping and calculation set a task of error, inaccuracy at simulation. In practice one applies by discreet process simulation let optimize similar function. If models is digital, (numerical data) at description by means of VHDL, to work is difficult of access if need to standard function width at most just to the original. For every discreet element et his model in any case use the concrete kind. For example; - to connected electrical elements in system present in one model else connected models.

Basic conception for description of digital electronic circuit scheme with electrical undone model is this en VHDL. This conception has an effect in many level of abstraction – from one logical element to total system hardware.

Models are abstract or materials system in spirit realization. This system reflected objects and be able to replacement. A reality object and replacement description is model. Make a study of information by object give norm for principal work models.

Models is categorize in differing indication, example: 1) by methods of reflection or else way re-create objects; 2) by methods of models work (law of the work); 3) by specific characteristic in original who investigate or reproduce in model e.t.c.

By experience in any case delay is important by each logical operation. From theirs reality reflects subjection originality result of simulation. Still more logical operations ought to one at this distance of time at delay of this operation

In terminology using this process of name mixed-signal, mixed-level, and multi-level (block, circuit, and device)

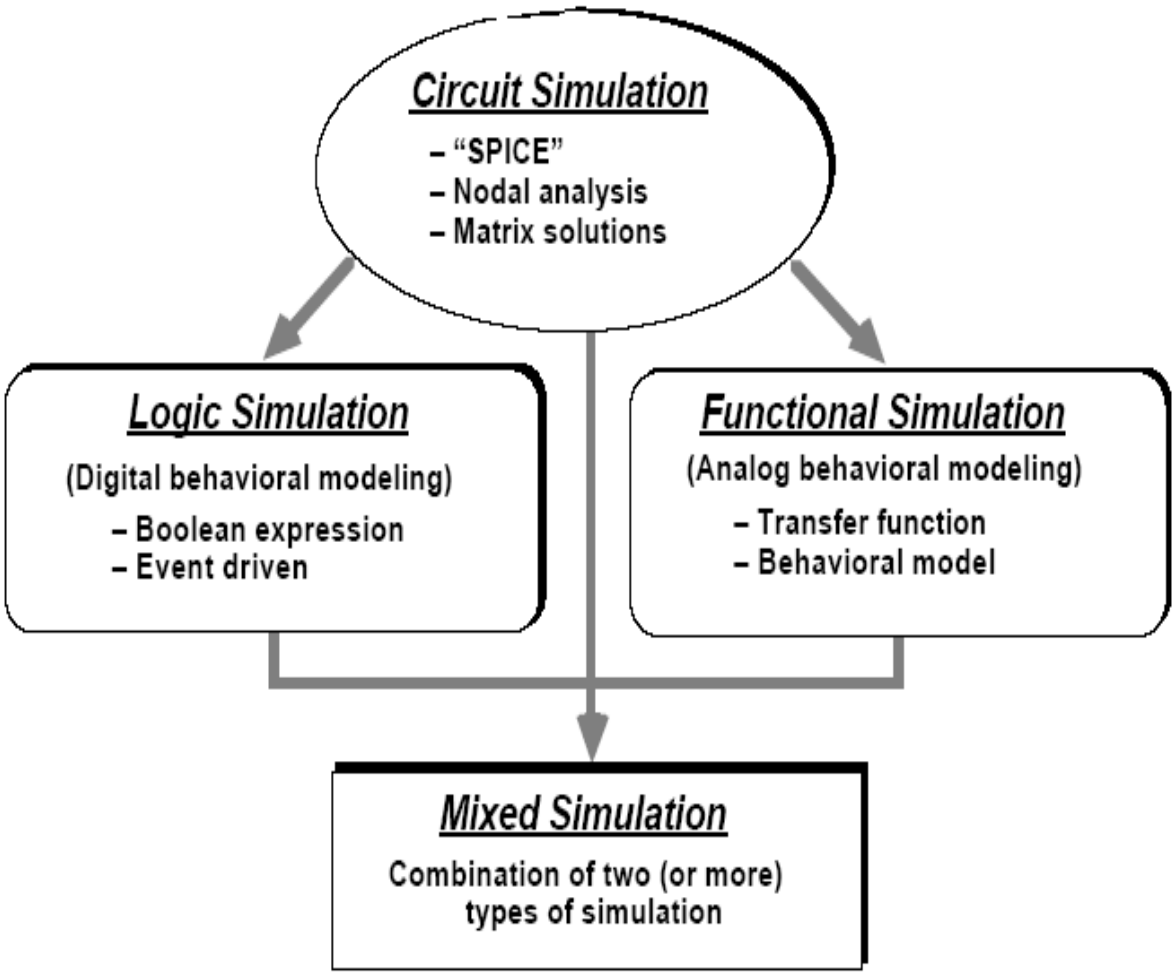
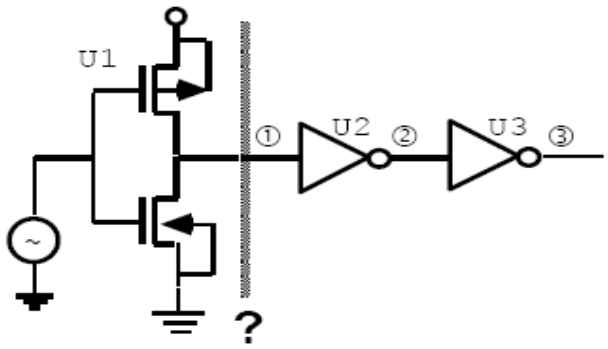


Fig.1. Type of simulation. Logical, functional and mixed



The mixed-mode scenario

- Which gate(s) should be simulated as "analog"? (*circuit partitioning*)
- When should it (they) be simulated as "analog"? (*mode switching*)

Fig 2. Interface in mixed simulation

Interface is define in two part presented in right front paper. Scenario is decide two problems, "problem of which, and problem of when. Logical element is presented in analog part and this part is decrypting in analog algorithm, et second part of digital element and this part is decrypting in other digital algorithm in digital simulation. Among two parts is creating the interface of transferring the parameters. Interface is important point of process transferring. On this process dependent the quality of work the models and simulators.

Approach resolves problems of multy-level presentation, automatic partition and dynamic switching in array of design. In based method mixed parameters of models in applications is scaling of array. For presented example tree is moment of using and correct parameter of models. Thesis is for one – using full "digital" mode for logic synthesis with vendor-supplied delay parameters and then Subcircuit model for back-annotated timing verification, for second – using "mixed" mode for data-converter systems witch large ratio of digital/analog circuitry (parts of mixed-signal interface circuits). Example touch problem of simulation in system-level e.t. large system with mixed digital gates and analog functional blocks.

Creating the interface in logical elements is presented in next point. In fig. 3. logical element of U1 gives of library simulator and look at his structure:

Logic element

```
U1 0 3 2 1 nmos nor2 nmos-nor2
```

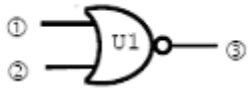


Fig. 3. Normal element of library

In reality position of placement the motherboard elements have included parameters com capacitance par example. These parameters are presented in fig. 4. Representation has digital, behavioral description and design scheme models.

Logic (digital, behavioral) representation

```
.model nmosnor2 logic vmax=1.0
+ vmin=0.1 thh=0.8 thl=0.2 mr=5
+ mf=5 over=0.1 cap1=… cap2=…
```

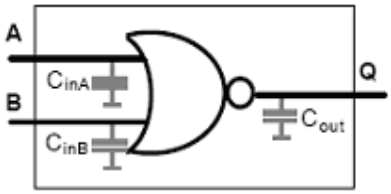


Fig. 4. Descript of reality element

The structure the element has decrypted between the analog methods. Structural circuit scheme is represented in fig. 5.

Circuit (analog, structural) representation

```
.subckt nmos-nor2 0 3 2 1
M1 3 1 0 nmos l=0.5u w=5u
M2 3 2 0 nmos l=0.5u w=5u
M3 4 3 3 nmos l=0.5u w=4u
Vdd 4 0 1.0
.ends
```

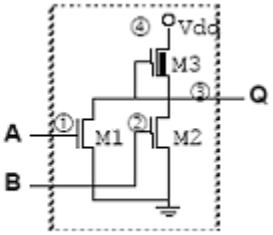


Fig. 5. Descript of structure the element

This way of presentation one element of digital simulators and analog models is very important between descript consist signals of structure element (analog signals) and functional digital signals of digital logic element. Simulation begins to analog and finish to digital. This manner is mixed simulation and level of signals – multy-level simulation. Fragment of code descript presented in fig.6.

```
Xsim=> fanout
 U1: c_fanout = 1.93372e-14
 U2: c_fanout = 6.1576e-15
 U3: c_fanout = 6.1576e-15
 U4: c_fanout = 6.67485e-15
 U5: c_fanout = 2.01527e-15
 U6: c_fanout = 2.11913e-15
 U7: c_fanout = 1.63416e-15
Xsim=> network u
Node: Branches:
   0: U1 U2 U3 U4 U5 U6 U7
   1: U1
   2: U1 U2 U5 U6 U7
   3: U2 U3
   4: U3 U4
   5: U4
   6: U5
   7: U6
   8: U7
Xsim=> network a
Node: Branches:
   0: A1.U1 A1.U2 A1.U3 A1.U4 A1.U5 A1.U6
A1.U7
   1: A1.U1
   2: A2.U1 A2.U1 A1.U1 A1.U2 A1.U5 A1.U6
A1.U7
   3: A2.U2 A2.U2 A1.U2 A1.U3
   4: A2.U3 A2.U3 A1.U3 A1.U4
   5: A2.U4 A2.U4 A1.U4
   6: A2.U5 A2.U5 A1.U5
   7: A2.U6 A2.U6 A1.U6
   8: A2.U7 A2.U7 A1.U7
Xsim=> network c
Node: Branches:
   0: C1
   1: Cgd.A1.U1 Cgs.A1.U1
   2: Cgd.A2.U1 Cgs.A2.U1 Cgd.A1.U2
+ Cgs.A1.U2 Cgd.A1.U5 Cgs.A1.U5
+ Cgd.A1.U6 Cgs.A1.U6 Cgd.A1.U7
+ Cgs.A1.U7
   3: Cgd.A2.U2 Cgs.A2.U2 Cgd.A1.U3
+ Cgs.A1.U3
   4: Cgd.A2.U3 Cgs.A2.U3 Cgd.A1.U4
+ Cgs.A1.U4
   5: Cgd.A2.U4 Cgs.A2.U4 C1
   6: Cgd.A2.U5 Cgs.A2.U5
   7: Cgd.A2.U6 Cgs.A2.U6
   8: Cgd.A2.U7 Cgs.A2.U7
Xsim=> network r
Node: Branches:
   0: Rs.A1.U1 Rs.A1.U2 Rs.A1.U3
+ Rs.A1.U4 Rs.A1.U5 Rs.A1.U6 Rs.A1.U7
   1:
   2: Rs.A2.U1 Rd.A1.U1
   3: Rs.A2.U2 Rd.A1.U2
   4: Rs.A2.U3 Rd.A1.U3
   5: Rs.A2.U4 Rd.A1.U4
   6: Rs.A2.U5 Rd.A1.U5
   7: Rs.A2.U6 Rd.A1.U6
   8: Rs.A2.U7 Rd.A1.U7
```

Fig. 6. Descript of code structure the element

In process simulation very important is subcircuit expansion approach, dynamic delay models and behavioral-level and block level modeling. Subcircuit expansion cont in circuit partition (BBD matrix) and logic gate model and automatic mode switching. In this case by example for mixed simulations in 4-bit ring counter et results is compare with 4-bit full ADDER (48 logic gates, 224 transistors).

Scheme of counter for example presented in fig.7., and net list and diagram view in fig. 8. and fig. 9. This example demonstrate equivalent of analog and digital simulation of special element. In this way is possibility transfer the parameters in one part to other. Important moment of statement is possibility of choice the algorithm of calculate the simulation. This choice is necessary in many moment of simulation where needed transfer the parameters or signals of different element (analog and digital).

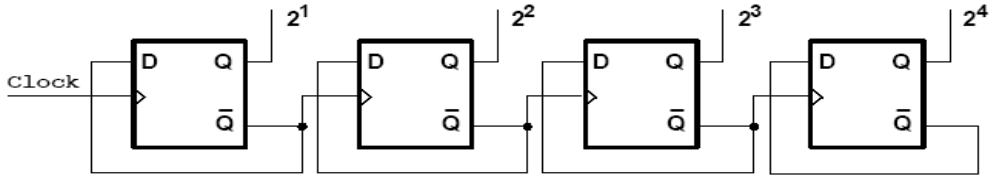


Fig. 7. Scheme of 4-bit ring counter in one element

Net list or diagram view two part from result the work of digital and analog simulation. Doddet line in fig.9. is work of digital model in digital simulator. Structure of ring element is presented in analog of fig.5.

Xsim Netlist

```
Xsim netlist for the shift register
.lib mos12u
X1 1 2 2 3 dff
X2 2 4 4 5 dff
X3 4 6 6 7 dff
X4 6 8 8 9 dff
.subckt dff 1 3 9 10
U1 0 5 6 3 4 cmos nand3 cmos-nand3
U2 0 6 7 1 5 cmos nand3 cmos-nand3
U3 0 7 8 1 4 cmos nand3 cmos-nand3
U4 0 8 2 5 7 cmos nand3 cmos-nand3
U5 0 10 2 7 9 cmos nand3 cmos-nand3
U6 0 9 10 6 4 cmos nand3 cmos-nand3
V_clear 4 0 5
V_preset 2 0 5
.ends dff
V_clock 1 0 pulse(5 0 0 0 0 10n 20n)
.options mode=digital
*.options mode=analog
.tran 0 200n 0.1n
```

Fig. 8. Net list code 4-bit ring

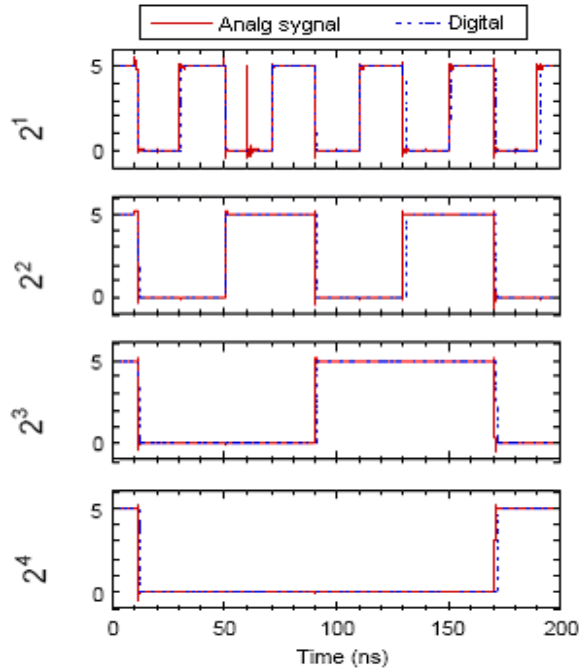


Fig. 9. Diagram of example

Different parameters is worked in capacitance circuit et parameter is transferring in capacitance environment.

2. CONCLUSION

Simulation is mixed when in process appear models in different part – analog and digital. This paper present simulation or simulators of different element et simulation is correctly independently of simulators. Part of analog and part of digital is equal the same form et process of simulation and algorithm is possibility choice. In scheme have analog and digital element. His model is various. Simulation of deferent model should specific method and algorithm for simulation. This presentation recommended simulation as a whole, whole process and different models.

The running process shows simulation and transferring. For example demonstrate combine simulation a whole. Correctly result possibility using for big scheme and design.

3. REFERENCES

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