VERIFICATION AND VALIDATION OF MULTIPLYING DIGITAL-TO-ANALOG CONVERTER MACROMODELS

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This paper describes the process of Spice-based macromodel verification and validation. Verification and validation checks have been performed on the new Spice compatible macromodel developed using an Analog Devices AD7533 Current Output Digital-to-Analog Converter (DAC) integrated circuit (IC). The verification process has been implemented by comparing simulation results with typical values from IC datasheets. The circuits for simulations are created following the test conditions given in the datasheets. The simulation testing of the macromodel is performed within EDA OrCAD. Parametric dc, ac and transient analyses are specified and performed during the process of Spice simulations. The global parameters for simulations were the electrical states of digital inputs of the DAC model. Comparison between macromodel and data sheets shows that the average error is not higher than 15%. The validation process of the model is important to check behavior of the equivalent circuit by comparison to the real system performance conditions. Three electronic circuits – programmable amplifier, waveform generator and programmable universal (Low-pass, High-pass, Band-pass, and Band-reject) active filter, in which are incorporated multiplying 4- quadrant DACs, are prototyped for the needs of the validation. These circuits also include precision JFET-input op amps AD712 and universal active filter UAF42 (Texas Instruments). In those electronic circuits the dominant electrical parameters, for example voltage gain, pole (center) frequency and rise time are defined by the state of the digital inputs of the DAC model. Comparison analysis between simulation results of the proposed model and experimental results of the electronic circuits shows that the error is within 15%, which guarantees the sufficient degree of accuracy.

1. MACROMODEL VERIFICATION

After completing modeling process is desirable and necessary to define what is/isn't modeled, plus a basic question of *model accuracy*. All these points are important, in order to place confidence in simulation results. So, *verification* process of the model is important to check behavior of each element or group of elements from equivalent circuit by comparison to the actual device performance conditions. The equivalent circuit needs to be verified in the lab, by breadboarding and prototyping. A breadboard circuit is a quickly executed mockup of the circuit design using a semi-permanent lab platform, i.e., one which is less than final physical form. It is intended to show real performance, but without the total physical environment. A good breadboard can often reveal behavior not predicted by PSpice, either because of an incomplete model, external circuit parasitics, or numerous other reasons. However, by using PSpice along with intelligent breadboarding techniques, a circuit can be efficiently and quickly designed with reasonably good assurance of working properly on a prototype version [8].

The verification of the new macromodel of the IC AD7533 presented in paper [3] is performed by comparison the simulation results for the electrical parameters with the

typical values from datasheets. The simulation testing of the macromodel is performed within EDA OrCAD [4]. During the process of PSpice simulations are specified and performed parametric dc, ac and transient analyses. The global parameters during simulation processes were the electrical states of digital inputs of the DAC model. The circuits for simulations are created following the test conditions given in the datasheets of the corresponding IC.

Following the methodology [1] in Table 1 are summarized the simulation results for the new macromodel AD7533/MOD. The comparison give a good agreement between the macromodel and the datasheet parameters, the resulting error is not higher than 15% which guarantees the sufficient degree of accuracy.

Table 1 Comparison of the AD7533/MOD macromodel with datasheets of the IC.
The following specifications applied for $U_{CC} = +15V$, $T_A = 25°C$ and $U_{REF} = +10V$.

№	Parameter	Conditions	AD7533 Datasheet (x_{DS})	AD7533/MOD Macromodel (x_M)	Error ($\delta^{(1)}, \%$)
Static accuracy					
1.	Resolution	-	10Bits	10Bits	-
2.	Gain Error	Digital Inputs HIGH	±1,4%	±1,2%	14,28%
3.	Output Leakage Current I_{OUT1} I_{OUT2}	Digital Inputs LOW, $U_{REF} = \pm 10V$ Digital Inputs HIGH $U_{REF} = \pm 10V$	±50nA max ±50nA max	±50,5nA max ±50,4nA max	1% 0,8%
Dynamic accuracy					
4.	Output Current Settling Time	$R_L = 100\Omega$, Digital Inputs HIGH to LOW or Digital Inputs LOW to HIGH	600ns max	550ns	8,33%
5.	Feedthrough Error	Digital Inputs LOW, $U_{REF} = \pm 10V$, 100kHz sine wave	±0,05% max	±0,052% max	4,6%
Reference input					
6.	Input Resistance	Digital Inputs HIGH	$10k\Omega$	$10,01k\Omega$	0,1%
Analog outputs					
7.	Output Capacitance C_{OUT1} C_{OUT2} C_{OUT1} C_{OUT2}	Digital Inputs HIGH Digital Inputs LOW	100pF max 35pF max 35pF max 100pF max	100pF max 35pF max 35pF max 100pF max	- - - -
Digital inputs					
8.	Input High Voltage U_{iHIGH}	-	2,4V min	2,39V	0,4%
9.	Input Low Voltage U_{iLOW}	-	0,8V max	0,79V	1,25%
10.	Input Leakage Current I_{in}	$U_{in} = 0V$ and U_{DD}	±1μA	±1μA	-
11.	Input Capacitance C_{in}	-	8pF max	8pF max	-

Power requirements					
12.	Supply Voltage U_{DD} Supply Current I_{DD}	All Digital Inputs HIGH or LOW	+15V 2mA max	+15V 1,99mA max	0,5%

Note 1: $\delta = [(x_{DS} - x_M)/x_{DS}].100\%$.

2. MACROMODEL VALIDATION

During the validation the performance of the AD7533 model has been compared against the real IC. Based on the data sheets of the AD7533 are prototyped three electronic circuits of programmable amplifier, waveform generator, and programmable active filter. The type of elements and test conditions are chosen in accordance with the IC data sheets [5] and the conditions given in [7, 9].

2.1. Programmable Amplifier with DAC

On the Fig. 3.1 is shown programmable amplifier including DAC model (presented as a hierarchical block HB_AD7533) connected in the feedback of the precision JFET – input op amp AD712 [5, 6]. In this way the voltage gain is defined by the state of the digital inputs (pin 4 to pin 13).

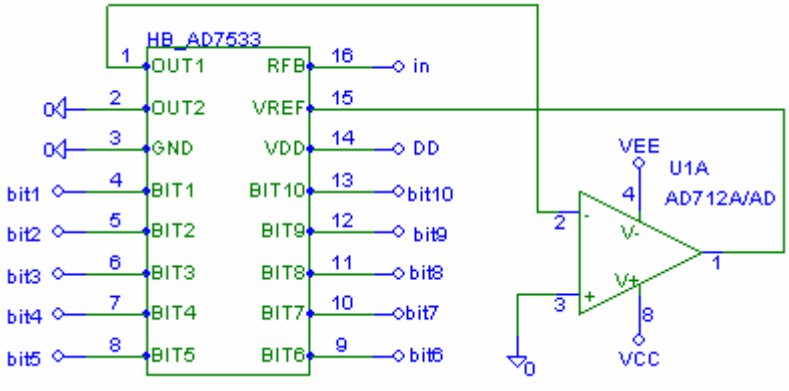


Fig. 3.1. Programmable Amplifier with DAC model AD7533.

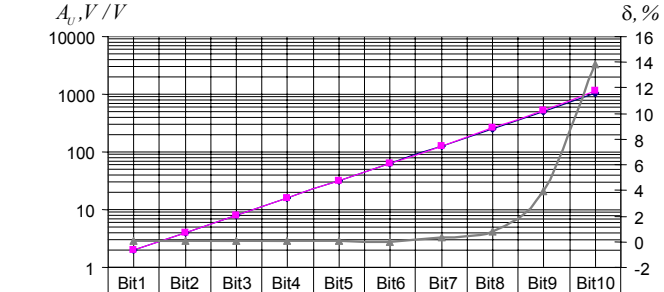
The transfer function of the circuits can be expressed as

(3.1) $A_U = \frac{U_o}{U_i} = -\frac{R + R_{on}}{R_F}\frac{2^{10}}{N}\frac{1}{1 + j\frac{f}{f_p}}$ where $f_p = \frac{N}{2\pi.2^{10}.(R + R_{on})C_k}$ is a pole frequency and $N = Bit10 + 2.Bit9 + 2^2.Bit8 + ... + 2^7.Bit3 + 2^8.Bit2 + 2^9.Bit1$ is a digital word.

We see that (3.1) voltage gain has changed between 1 and 1024, if N changed from 1 to 1024. The op amp AD712 is presented in the standard PSpice libraries with third level of complexity macromodel [1, 2]. The op amp model reflected all first order effects and some of the second order effects; including input offset voltage/currents, differential and common mode input capacitances, multiple pole-zeros, etc. Following the simulation testing methodology for the op amp macromodel AD712 is obtained open-loop voltage gain $A_d = 103dB$ $(141253V/V)$ and unity gain bandwidth $BW = 4{,}49MHz$. As well as the voltage gain slope is $20dB/dec$. It is seen that the simulation results compare closely with datasheets of the real IC [6]. For the simulation testing of the programmable amplifier is planed and preformed ac analysis with the following sweep parameters: point per decade 100; start frequency $0{,}1Hz$; end frequency $10MHz$. PSpice simulations are implemented for a ten values of the digital inputs, namely $Bit1 = "1"$ $(A_U = 2)$, $Bit2 = "1"$ $(A_U = 4)$, etc. The input signal of the circuit is connected to pin 16 of the Data Converter and have 10mV amplitude and zero ac phase. For the physical experiments of

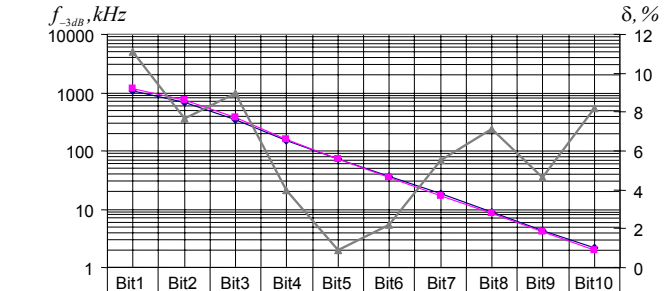
the real electronic circuit the input signal is received from sinusoidal generator with frequency range 0,1Hz -10MHz and output resistance 50Ω.

On the Fig. 3.2a and Fig. 3.2b are presented simulation output ($A_{U,M}$ - voltage gain and $f_{-3dB,M}$ - bandwidth), experimental results ($A_{U,Exp}$ and $f_{-3dB,Exp}$) and error in percents ($\delta = \left[\left(x_{,M} - x_{,Exp}\right)/x_{,M}\right]100\%$) versus digital input states. In the tables below (Fig. 3.2a and Fig. 3.2b) are given numerical values for the amplifier parameters, simulation results and errors. The comparison gives a very good agreement between the macromodel created and the real DAC circuit, the resulting error being within 15%.



	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10
$A_{U,Exp}$	2	4	8	16	32	64	128	256	512	1024
$A_{U,M}$	2,002	4,004	8,008	16,01	32,03	64,01	128,4	258	532	1166
δ, %	0,1	0,097	0,094	0,087	0,094	0,016	0,297	0,781	3,906	13,87

Fig. 3.2a. Comparison of the model and experimental results for the voltage gain A_U.



	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10
$f_{-3dB,Exp}$	1080	690	346	150	72	36,6	18,12	9,1	4,3	2,2
$f_{-3dB,M}$	1200	743	377	156	72,66	35,8	17,12	8,45	4,1	2,02
δ, %	11,11	7,681	8,96	4	0,917	2,186	5,519	7,143	4,651	8,182

Fig. 3.2b. Comparison of the model and experimental results for the bandwidth f_{3dB}.

2.2. Waveform Generator

The second electronic circuit of a programmable waveform generator, used for validation of the new model is represented on Fig. 3.3 [5]. The generator includes programmable integrator and Schmitt trigger (comparator) with global feedback. For the realization of the integrator and Schmitt trigger is used JFET – input op amp AD712. The potentiometer R_ρ is for calibration of the output frequency. The amplitude of the output signal is define by the Zener diodes D_1 and D_2. The threshold voltage of the comparator and output voltage of the integrator is given as

$$U_p = -\frac{R_1}{R_2}U_{out1}; \qquad U_{out2} = -\frac{1}{C(R+R_{on})}U_{ref}\frac{N}{2^{10}}t + U_{out2}(0).$$

It can be seen that the output voltage of the integrator is changed linear versus time. The sign of the reference voltage U_{ref} are changed by the variation of the output voltage U_{out1}. Therefore the slew rate of the U_{out2} is defined by the time constant $\tau = (R + R_{on})C$, the reference voltage U_{ref} and the digital word

$$(3.3) \qquad \frac{dU_{out2}}{dt} = -\frac{1}{(R+R_{on})C}\frac{N}{2^{10}}U_{ref} \approx -\frac{1}{RC}\frac{N}{2^{10}}U_{ref} \text{ where } R >> R_{on}.$$

Then the output frequency of the circuit can be expressed as

$$(3.4) \qquad f_o = \frac{1}{4RC}\frac{N}{1024}\frac{R_p^{'}}{R_\rho^{'} + R_p^{''}}.$$

It can be seen that the frequency of the output signal is linear function of word *N*.

The verification of the waveform generator is implemented by comparison analysis between PSpice simulations and physical experiments. For the PSpice simulations are

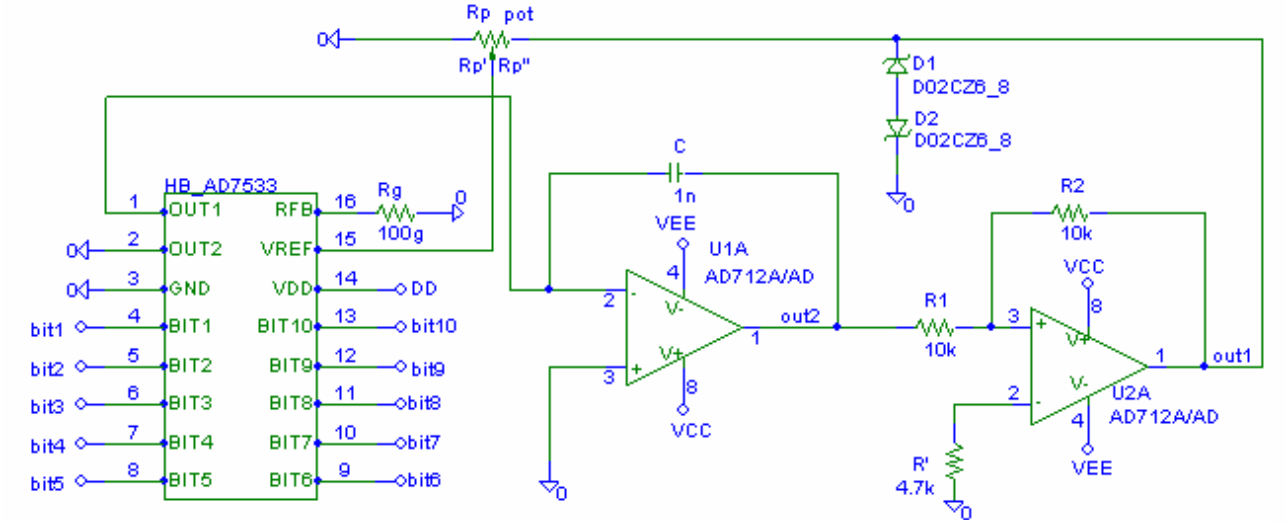
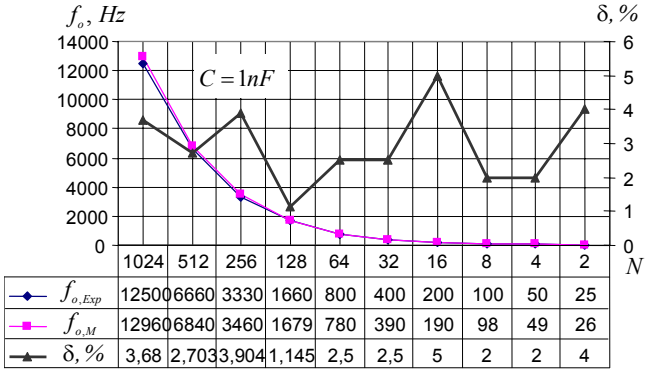


Fig. 3.3. Waveform Generator with current output DAC AD7533.

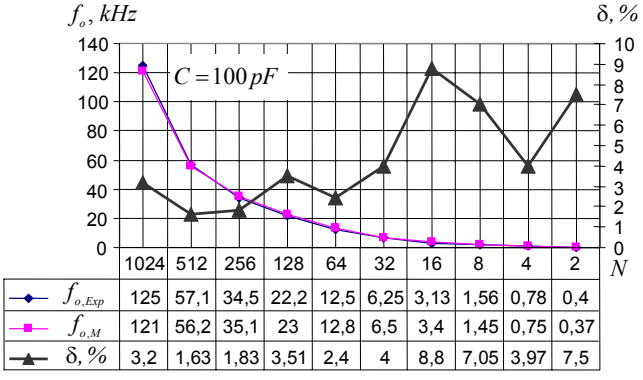
performed parametric transient analysis. The global parameter during the simulations is the digital word N with values 2, 4, 8, 16, etc. During the physical experiments the shape, amplitude and frequency of the rectangular and triangular signals are measured with oscilloscope and multimeter. Supply voltages for the circuit are $\pm 15V$.

On the Fig. 3.3a and Fig. 3.3b are presented simulation output, experimental results for the output frequency f_o and error in percents at $C = 1nF$ and $C = 100\,pF$ versus the digital input states. The numerical values of the two portions of the potentiometer R_ρ are: $R_p^{"} = 4{,}36k\Omega$ and $R_p^{'} = 14{,}5k\Omega$. In the tables below (Fig. 3.3a and Fig. 3.3b) are given numerical values for the amplifier parameters, simulation results and errors. Again, it is seen that the comparison is very close ($\delta < 10\%$). The real test of the waveform generator at $C = 100\,pF$ and $N = 1023$ show that the rise time of the output signal is 664ns. During the PSpice simulations of the same circuit the rise time is 600ns, which guarantee the correct degree of accuracy ($\delta < 9{,}6\%$).



N	1024	512	256	128	64	32	16	8	4	2
$f_{o,Exp}$	12500	6660	3330	1660	800	400	200	100	50	25
$f_{o,M}$	12960	6840	3460	1679	780	390	190	98	49	26
δ, %	3,68	2,703	3,904	1,145	2,5	2,5	5	2	2	4

Fig. 3.3a. Comparison of the model and experimental results for f_o at $C = 1nF$.



N	1024	512	256	128	64	32	16	8	4	2
$f_{o,Exp}$	125	57,1	34,5	22,2	12,5	6,25	3,13	1,56	0,78	0,4
$f_{o,M}$	121	56,2	35,1	23	12,8	6,5	3,4	1,45	0,75	0,37
δ, %	3,2	1,63	1,83	3,51	2,4	4	8,8	7,05	3,97	7,5

Fig. 3.3b. Comparison of the model and experimental results for f_o at $C = 100\,pF$.

2.3. Programmable Active Filter

The third electronic circuit which is used to validate the proposed DAC model is programmable active filter (Fig. 3.4) [7]. The circuit include universal active filter UAF42 (Texas Instruments) and two programmable integrators with current output DAC AD7533. The pole frequency of the filter is controlled by changing the time constant of the integrators. The circuit realized second order Low-pass, High-pass, Band-pass and

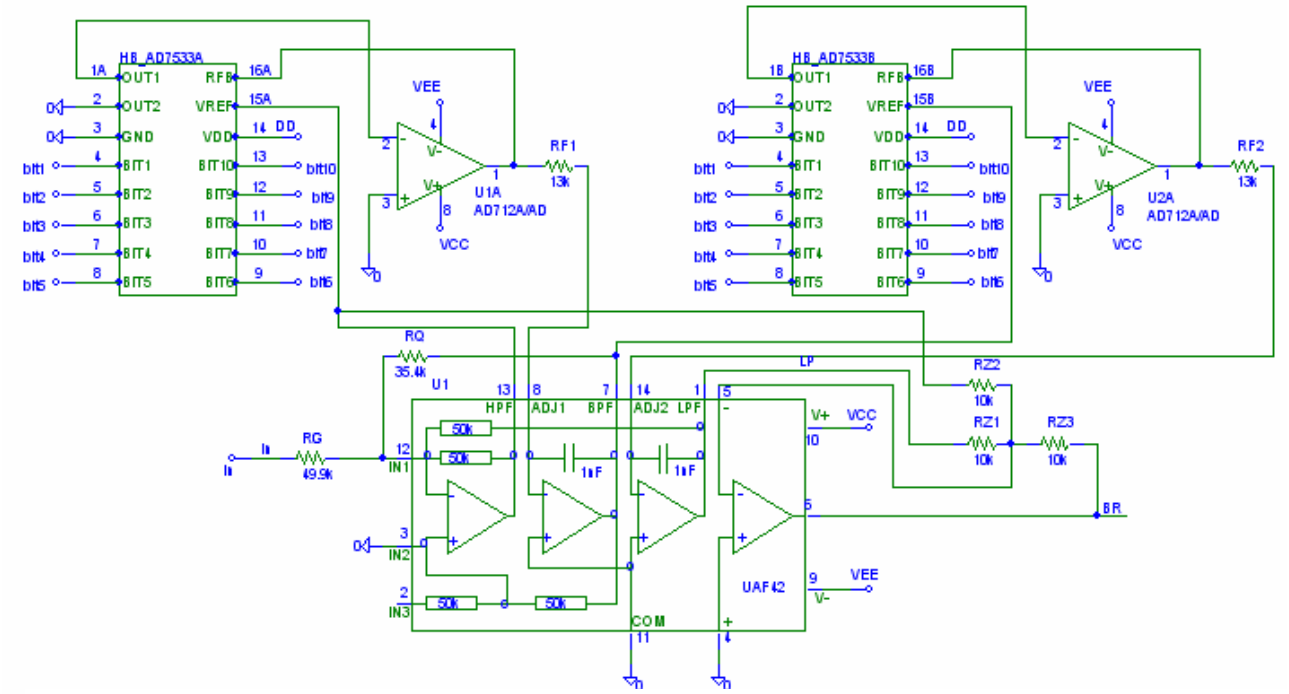


Fig. 3.4. Programmable Active Filter

Band-reject transfer functions. The pole (center) frequency is given as

$$(3.5)\qquad f_p = \frac{1}{2\pi R_F C}\frac{R_{FB}}{(R+R_{on})}\frac{N}{1024} \approx \frac{1}{2\pi R_F C}\frac{N}{1024} \quad \text{where} \quad R_{FB} \approx R + R_{on}\ \ (R >> R_{on}),$$

and $R_F = R_{F1} = R_{F2} = 13k\Omega$. The Q-factor of the active filter can be expressed as

$$(3.6)\qquad Q_\rho = R_Q\sqrt{\frac{1}{R_1 R_2}} = 0{,}708 \ \text{ where } \ R_Q = 35{,}4k\Omega \pm 1\% \ \text{ and } \ R_1 = R_2 = 50k\Omega \pm 1\%$$

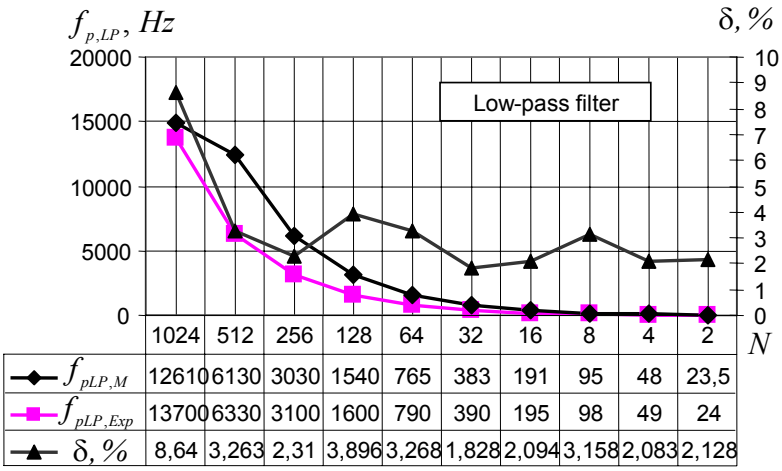
(internal elements of the real IC).

Verification of the filters is performed in the same manner as a programmable amplifier. For the PSpice simulations are performed parametric ac analyses. The input signal is obtained from a sinusoidal generator with altering frequency. The simulations are implemented for a ten values for the digital word, namely $Bit10 = "1"$, $Bit9 = "1"$, etc.

On the Fig. 3.5a, Fig. 3.5b and Fig. 3.5c are presented simulation output, experimental results and error in percents for the pole (center) frequency versus digital input states. The comparison gives a good agreement between the model and the real DAC circuit, the resulting error is not higher than 12%.

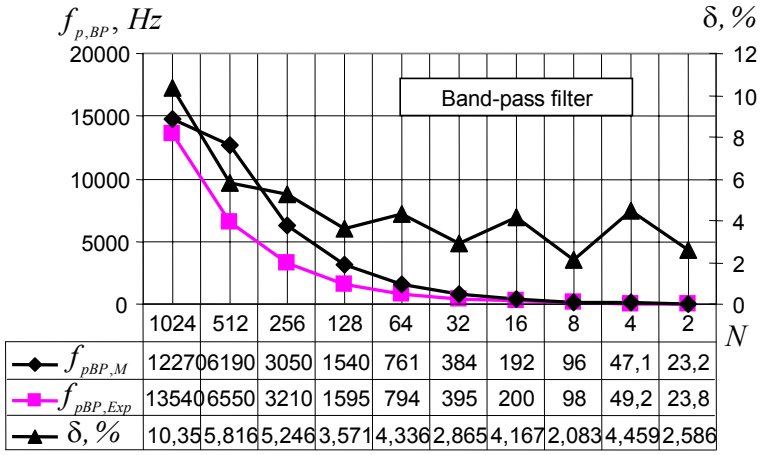
3. CONCLUSIONS

In this paper verification and validation processes of the new PSpice macromodel for commercial IC Digital-to-Analog Converters have been presented. Comparison between



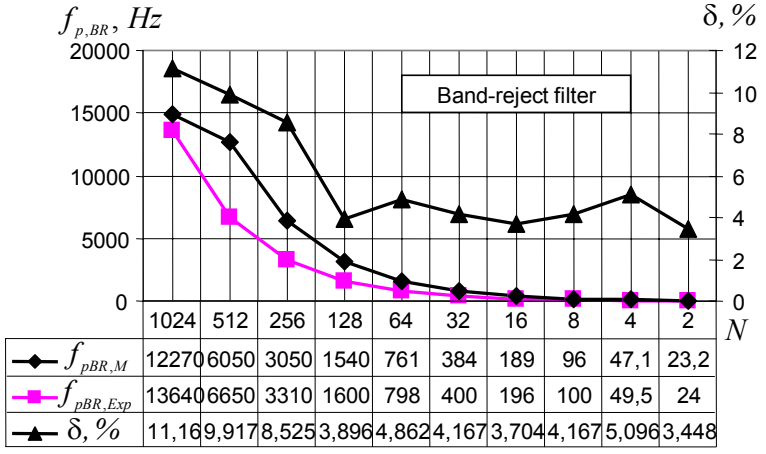
N	1024	512	256	128	64	32	16	8	4	2
$f_{pLP,M}$	12610	6130	3030	1540	765	383	191	95	48	23,5
$f_{pLP,Exp}$	13700	6330	3100	1600	790	390	195	98	49	24
δ, %	8,64	3,263	2,31	3,896	3,268	1,828	2,094	3,158	2,083	2,128

Fig. 3.5a. Comparison of the model and experimental results for the Low-pass filter



N	1024	512	256	128	64	32	16	8	4	2
$f_{pBP,M}$	12270	6190	3050	1540	761	384	192	96	47,1	23,2
$f_{pBP,Exp}$	13540	6550	3210	1595	794	395	200	98	49,2	23,8
δ, %	10,35	5,816	5,246	3,571	4,336	2,865	4,167	2,083	4,459	2,586

Fig. 3.5b. Comparison of the model and experimental results for the Band-pass filter



N	1024	512	256	128	64	32	16	8	4	2
$f_{pBR,M}$	12270	6050	3050	1540	761	384	189	96	47,1	23,2
$f_{pBR,Exp}$	13640	6650	3310	1600	798	400	196	100	49,5	24
δ, %	11,16	9,917	8,525	3,896	4,862	4,167	3,704	4,167	5,096	3,448

Fig. 3.5c. Comparison of the model and experimental results for the Band-reject filter

the new models and IC data sheets provided by the manufacturers for the main dc and ac electrical parameters show that the average error is not higher than 15%, which guarantee sufficient degree of accuracy.

With the proposed macromodel, the designer can quickly determine the dominant effects of the electronic circuits include data converters that are difficult to obtain with breadboarding.

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