MULTIPLYING DIGITAL-TO-ANALOG CONVERTER MACROMODELS DEVELOPMENT

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This paper discusses the design of Spice-based macromodels for current output multiplying Digital-to-Analog Converter (DACs). Implementation of the macromodel is based on simplifycation and build-up methods. The structure of the equivalent circuits consists of R-2R ladder, voltage-controlled switches, ideal sources represent input (output) leakage currents, and capacitors reflect input and output capacitance. This configuration, with a suitable choice of technologies and elements, accurately models width range of multiplying Digital-to-Analog Converters using current-scaling architecture. The macromodel presented here reflects the full functional and logical behavior of the real devices. The model represents static and dynamic modes of operation and the corresponding parameters: gain error, output (input) leakage current, current settling time, bandwidth, feedthrough attenuation ratio, input resistance, output capacitance, digital input high and low threshold voltages and power dissipation in a quiescent state. The macromodel are not yet capable of simulating thermal effects, noise, parametric variation (the model do not include Monte Carlo parameters so statistical analysis of circuit performance due to lot and device variation is not available), parasitic effects of device package, etc.

1. INTRODUCTION

The ability to convert digital signals to analog and vise versa is very important in signal processing. In the Digital-to-Analog Converters (DACs) digital words are applied to the its input to create from a reference voltage an analog output signal that is a representation of the digital word.

DACs are widely used in communication, instrumentation and medical systems to modify the dynamic range of a signal. They can be found in, e.g. programmable amplifiers, attenuators, waveform generators, programmable filters, oscillators, etc.

Many techniques have been used to implement DACs. In the contemporary electronic systems to design DACs there are three approaches that are compatible with integrated circuits technologies. These methods are current-scaling, voltage-scaling and charge-scaling [5, 8]. Current-scaling is widely used with BJT and MOS technology, whereas voltage- and charge- scaling are only for MOS technology.

Today the leading companies (Analog Devices [6], Maxim/Dallas Semiconductor [9], Texas Instruments [10], etc.) offer a variety of 8-bit to 16-bit current output DACs with serial and parallel interface. The Spice-based libraries overview shows the lack of macromodels for DACs in the professional ECAD systems. EDA OrCAD PSpice only provides two primitives to model analog-to-digital and digital-to-analog converters [3]. These two primitives simplify the modeling of these complex mixed-signal devices. The DAC primitive is a zero impedance voltage source from output

node to ground and a resistance between reference node and ground is 1/GMIN. This primitive represent only an ideal transfer function and typical value of switching time. In response of these problems the author proposes Spice-compatible macromodel for the circuit output multiplying DAC. The new macromodel accurately predict dc, ac, and transient performance behavior.

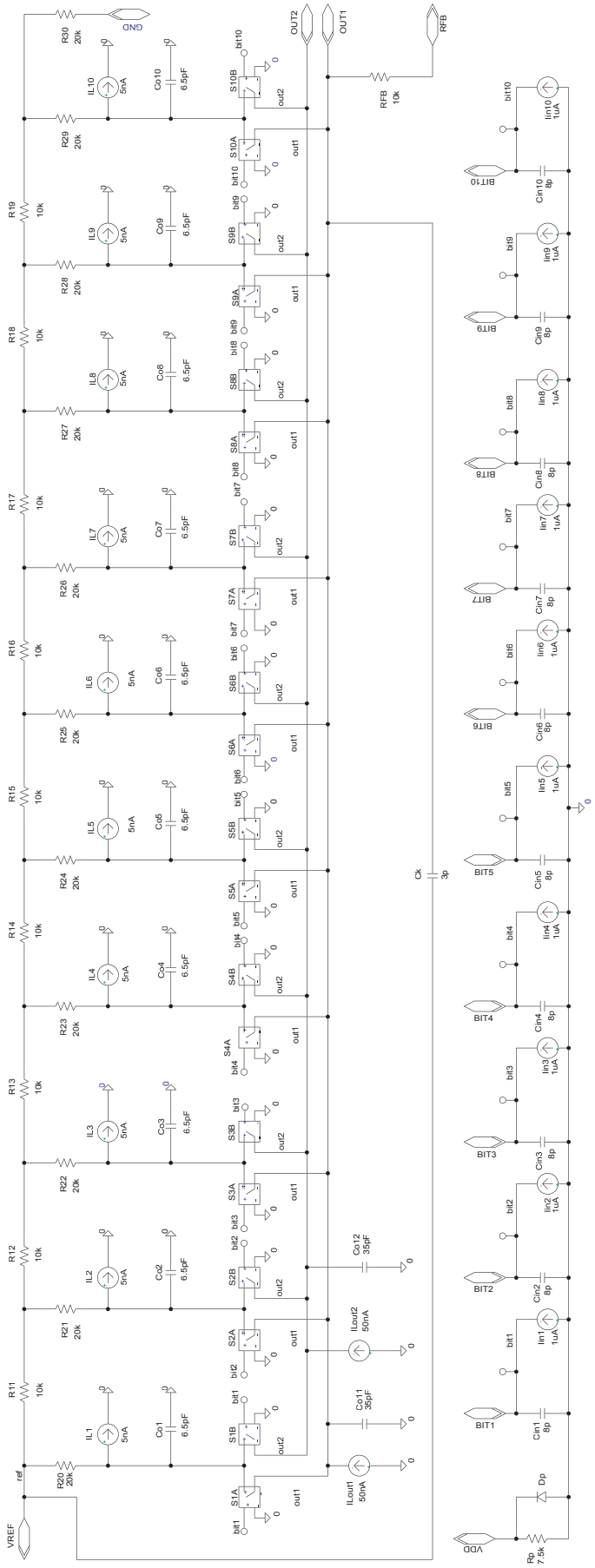

Fig. 1. Equivalent circuit of the multiplying DAC macromodel.

2. MACROMODEL DEVELOPMENT

The macromodel has been developed using two basic macromodeling techniques: simplification and built-up [1]. In the simplification techniques, representative portions of DAC are successively simplified by using simple ideal elements to reduce numerous real elements. In the built-up technique, a circuit configuration composed of ideal elements (voltage or current sources, resistors capacitors, etc) is proposed two meet certain electrical characteristics without necessary resembling a portion of an actual DAC circuit configuration.

The DAC used as an example of this paper is AD7533 IC [7]. This is a standard 10-bit 4-quadrant multiplying DAC integrated circuit manufactured using an advanced thin-film-on-monolithic CMOS wafer fabrication process. It contains R-2R

ladder and ten CMOS current switches on a monolithic chip. Most applications with AD7533 require an output operational amplifier.

The equivalent circuit of the proposed macromodel are shown in Fig. 1. The configuration, with a suitable choice of technologies and elements, accurately models width range of multiplying 4-quadrant Digital-to-Analog Converters using those architectures. For a given DAC, the macromodel provide an essentially pin-for-pin correspondence with real device, and accurately represents all functional and logical behavioral of the ICs, including dc and ac performance.

In the macromodel an inverted R-2R ladder structure is used – that is, binary weighed currents are switched between the I_{out1} and I_{out2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. In the circuit each CMOS current switch is presented with a two voltage-controlled switches labeled respectively with *A* and *B*. If the *i*th bit is 1 each switch from section *A* is connected to *out*1 ("ON") and each switch from section *B* is connected to *out*2 ("ON") if the *i*th bit is 0. Obviously, the current from first leg (I_1) is equal to $Vref/2R$. The circuits $I_1, I_2, I_3, \ldots, I_n$ are binary-weighted and given as

(1) $I_1 = 2I_2 = 4I_4 = \ldots = 2^{n-1} I_{n-1}$, where n is a resolution of the DAC.

Thus, the output current of the R-2R DAC of the Fig. 1 is given by

(2) $$I_{out1} = \frac{1}{R}\frac{U_{ref}}{2^n} N$$

where

(3) $N = Bit\ n + 2.Bit\ (n-1) + \ldots + 2^{n-2}.Bit2 + 2^{n-1}.Bit1$ – digital word.

For the AD7533 model $n = 10$ then Eq. 3 is modified as

$$N = Bit10 + 2.Bit9 + 2^2.Bit8 + \ldots + 2^7.Bit7 + 2^8.Bit2 + 2^9.Bit1.$$

According to the datasheet of the AD7533 [7] the resistors from R-2R ladder structure is $R_{11} = R_{12} = \ldots = R_{19} = R = 10k\Omega$ and $R_{20} = R_{21} = \ldots = R_{30} = 2R = 20k\Omega$.

To convert output current to voltage in addition of the DAC macromodel is necessary to connect output operational amplifier. In Fig. 2 is shown data converter with the output JFET op amp AD712 connected as current to voltage converter.

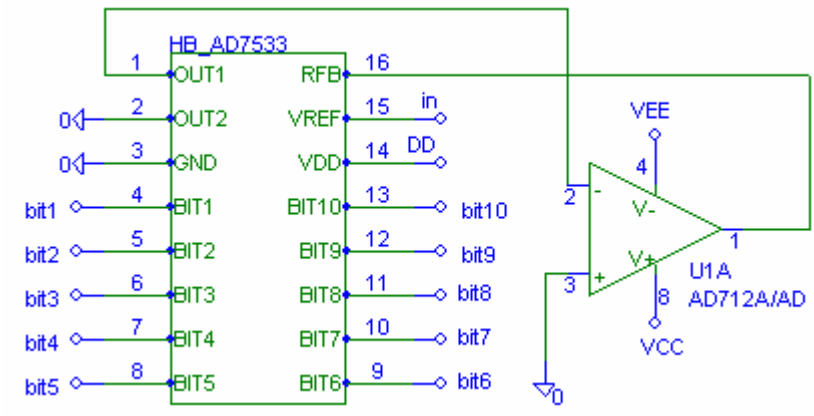

Fig. 2. DAC model AD7533 with output JFET op amp AD712.

AD7533 DAC model is presented as a hierarchical block HB_AD7533. Thus, the output voltage of the amplifier can be expressed as

(4) $$U_{out} = -\frac{R_{FB}}{R}\frac{N}{2^{10}} U_{ref},$$

where $R_{FB} = 10k\Omega$ is a feed-back resistor defining sca-ling factor of the circuit [7].

The *"ON" resistances*

of the real switches of the IC are modeled by the *RON* parameters of the voltage-controlled switches of the macromodel. According to the data sheets the *"ON" resistances* are binary scaled so the voltage drop across each switch is the same. Switch $S1A$ ($S1B$) of Fig. 1 was designed for an "ON" resistance of 20Ω, switch $S2A$ ($S2B$) for 40Ω, and so on. If the reference input is 10V, the current through switch $S1A$ ($S1B$) is 0,5mA, the current through $S2A$ ($S2B$) is 0,25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binary weighted current division property of the ladder is to be maintained.

When all switches from section *A* are "OFF" (all digital inputs are LOW) there also is some penetration of the input analog signal U_{ref} towards the circuit output through the switches. *Feedthrough attenuation* (*FA*) is the ratio of the output signal to the input signal in percents when all switches from section *A* are "OFF" [2, 4]. In the equivalent circuit the *FA* is modeled with the *ROFF* parameters of the switches from section *A*. The numerical value of *ROFF* can be calculated with:

$$ROFF = \frac{R_{FB} - R.FA}{FA}, \tag{5}$$

where FA is a feedthrough attenuation for a given frequency of the input signal and *R* is resistance from R-2R ladder structure.

According to equation (5) the value of $ROFF$ (Fig. 1) for AD7533 are $20M\Omega$ at $FA = 500.10^{-6}$ $(0{,}05\%)$, $U_{ref} = 10V$, $f_{ref} = 100kHz$ (sine wave), and $R = 10k\Omega$. The *"OFF" resistances* are binary scaled so the voltage drop across each switch is the same. Switch $S1A$ ($S1B$) of Fig. 1 was designed for an "OFF" resistance of $40M\Omega$, switch $S2A$ ($S2B$) for $80M\Omega$, and so on.

An important enhancement to the proposed DAC macromodel is the ability to realistically present *leakage current* $I_{Leakage}$ of the circuit. This current appears on *out*1 terminal when all digital inputs LOW or on *out*2 terminal when all inputs are HIGH. To aid this task, the DAC macromodel includes ideal current sources I_{L1} to I_{L10} connect in parallel to each leg of the R-2R ladder and two sources I_{Lout1} and I_{Lout2} connected to the *out*1 and *out*2 terminals. The values of $I_{Lout1} = 50nA$ and $I_{Lout2} = 50nA$ are obtained from the specifications [7] of the real IC. The current sources from I_{L1} to I_{L10} be chosen equal to -5nA. Then the output leakage currents can be expressed as

$$I_{Leakage1} = I_{Lout1} + \sum_{i=1}^{10} I_{Li} \tag{6a}$$

and

$$I_{Leakage2} = I_{Lout2} + \sum_{i=1}^{10} I_{Li} \,. \tag{6b}$$

Thus, when all digital inputs are HIGH the output leakage current $I_{Leakage1} = I_{Lout1} + \sum_{i=1}^{10} I_{Li} = 50.10^{-9} + \left(-50.10^{-9}\right)$ in terminal *out*1 will be zero and the current in terminal *out*2 will $I_{Leakage2} = I_{Lout2} = 50.10^{-9} A$ (current sources $I_{L1} \ldots I_{L10}$ are not connected to *out*2 when all digital inputs are HIGH).

The settling time is the period for the output function of the DAC to settle to within $\frac{1}{2} LSB$ for a given digital input stimulus. In AD7533 IC the main factors affecting the settling time are two. The first one is the time constant $\tau \geq (RON + R).(C_k + C_{out1})$, where C_k is the internal feedback capacitor and C_{out1} is the output capacitance (capacity from *out*1 to ground). The second factor is the maximum slew rate which can be received by the output amplifier connected as current to voltage converter.

According to the data sheets of the AD7533 when all inputs are HIGH the maximum output capacity from *out*1 to ground is $C_{out1} = 100 pF$ and from *out*2 is $C_{out2} = 35 pF$. The *output capacitances* of the modeled DAC is provided by ideal capacitors C_{o1} to C_{o10} connected parallel to each leg of the ladder and two capacitors C_{o11} and C_{o12} connected to the *out*1 and *out*2 terminals. The values of $C_{o11} = 35 pF$ and $C_{o12} = 35 pF$ are obtained from the electrical specifications of the integrated circuit [7]. The capacitors C_{o1} to C_{o10} be chosen equal to 6,5pF. Thus, when all digital inputs are HIGH the output capacitance in terminal *out*1 is

(7a) $$C_{out1} = C_{o11} + \sum_{i=1}^{10} C_{0i} = 35.10^{-12} + 65.10^{-12} = 100 pF$$

and the capacitance in terminal *out*2 is

(7b) $$C_{out2} = C_{o11} = 35 pF .$$

The bandwidth ($BW_{0,7}$) and *FA* versus frequency of the DAC is produced with the internal feedback capacitor C_k connected between *Vref* and *out*1 of the equivalent circuit. The numerical value of C_k can be calculated with:

(8) $$C_k = \frac{1}{2\pi BW_{0,7} 2R}.$$

The controlling circuit of the DAC is modeled with voltage-controlled switches $S1A$ ($S1B$) to $S10A$ ($S10B$), ten ideal current sources *Iin*1 to *Iin*10 mimic the *input leakage currents* and ten capacitors *Cin*1 to *Cin*10 presents *input capacitances*. *The input high and low voltages* are modeled by parameters VON (control voltage for "ON" state) and VOFF (control voltage for "OFF" state) of the switches. In the proposed macromodel the digital control inputs are TLL/CMOS compatible. The numerical values of the VON and VOFF parameters are obtained from the datasheet of the real IC.

To model the actual *dc power dissipation* of a DAC, a resistor R_P is introduced into the macromodel. For the circuit of Fig. 1, in a quiescent state, the power dissipation is $U_{DD} = I_{DD} R_P$. The necessary value of R_P to produce this dissipation depends on supply voltage U_{DD} and maximum quiescent current I_{DD} when all digital inputs are LOW or HIGH. The ideal diode D_P connected between VDD node and ground mimics the behavior of the macromodel if the polarity of the supply voltages is changed.

3. CONCLUSIONS

In this paper, new macromodel of the current output multiplying DACs is proposed. The macromodel make it possible to simulate electronic circuits (for example programmable amplifiers, filters, waveform generator, etc.) including DACs without significant increasing of simulation time and computer resources. In the process of implementation of the model are applied simplification and build-up methods. The developed equivalent circuit of the new macromodel, with suitable choice of elements and parameters, can be realistically models a broad class of Data Converters using current-scaling architecture. The macromodel presented are accurate enough for general circuit analysis and model the most important DAC transient, dc and ac characteristics and the corresponding parameters: gain error, output (input) leakage current, output current settling time, bandwidth, feedthough attenuation ratio, input resistance, input/output capacitance, digital input high (low) threshold voltages and power dissipation in a quiescent state.

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4. REFERENCES

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