COMPUTER BASED DESIGN OF A LOW FREQUENCY POWER AMPLIFIER

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This paper presents a computer-based design method for a low frequency power amplifier. This design method is based on an Excel workbook and is utilized basically for verifying the projects of the electrical engineering students, at the discipline "Electronic Devices and Circuits". The typical case is considered for the device values and characteristics in order to focus the student attention on the functioning principles. The basic calculus for each project can be found on one line of the first worksheet. A simplified analysis of the transistor characteristics was implemented (for the usually power transistors) and some systematic procedures for choosing the transistors were developed. Advanced calculations, about the harmonic distortion and frequency analysis, are made in the second worksheet.

1. INTRODUCTION

The project theme for the electrical engineering students is to design an audio power amplifier for certain specifications: the nominal output power ($P_{on}=5...80W$), the load resistance ($R_L=3...10\Omega$), the lower and upper 3-dB frequencies, the total harmonic distortion factor (THD) and the maximum ambient temperature (Ta). The intervals for the input sensitivity and for the input resistance are also known.

A three stages classical power amplifier, with the block diagram presented in figure 1, was considered. The class AB final stage (FS) is implemented with a complementary pair of power (or power Darlington) transistors, connected as emitter-followers and biased by a V_{BE} multiplier (VS). The driver stage (DS), a class A, large-signal amplifier, consists of a common-emitter transistor. A simple one transistor input stage (IS) has been considered in this paper. The overall negative feedback (NF) determines the voltage gain value and reduces significantly the THD factor.





2. THE CIRCUIT AND THE DESIGN PROCEDURE

Figure 2 presents the schematics of the power amplifier. The high frequency limit is determined by C3; this compensation circuit is very simple, with lack of amplifier performances in the high frequency domain. The high voltage gain in the driver stage is achieved by utilizing the Bootstrap connection at the final stage input.

For the design, the typical component parameters were considered, in order to focus the student attention on the working principles of the circuit. Later on, the top students can made the worst case analysis as in the real life design procedures.

Considering the specifications given for the project, the design must be conducted from the final stage through the input stage.

2.1 Choosing the final transistors - theory

The first goal is to find a systematic method for choosing the final transistors of the amplifier. When selecting the final stage transistors, the voltage, current and power ratings of the power transistor are used. The nominal peak output voltage and current, V_{op} and I_{op} , and the power supply voltage V_{CC} are:

$$P_{on} = \frac{V_{op}^2}{2R_{\rm L}}, \quad V_{op} = k_{vn} \frac{V_{CC}}{2}, \quad V_{CC} = \frac{\sqrt{8P_{on}R_{\rm L}}}{k_{vn}} \quad \text{and} \quad I_{op} = \frac{V_{op}}{R_{\rm L}}.$$
 (1)

The maximum power dissipated in one transistor of the final stage is [1]:

$$P_{dF\max} = \frac{2}{\pi^2} \frac{\left(V_{CC}/2\right)^2}{2R_L} \cong 0.2P_{o\max}, \qquad \text{(for } \frac{\partial P_{dF}}{\partial V_{op}} = 0\text{)}, \qquad (2)$$

where $P_{o\max}$ is the maximum output power (theoretical value, for a sine wave).

The theoretical conditions for choosing the final stage transistors are:

$$V_{CE0} > V_{CC}, \qquad I_{CM} > I_{op}, \qquad P_{tot} > P_{dF \max},$$
(3)

where the quantities written by normal letters (not italic) are the maximum ratings taken from the transistor data-sheet. The total power for a transistor (Ptot) has only a theoretical meaning, in practice a more reduced value should be considered in order to have a normal heatsink. This value can not be found directly because it depends on electrical, mecanical and thermical quantities. In order to choose the transistors algorithmically, this reduced power should be found (for typical conditions).

2.2 The maximum power dissipation of a power transistor

In equipment, the maximum power dissipation of a transistor is limited by the thermal resistance junction-heatsink plus thermal resistance heatsink-ambient and not only by the thermal resistance junction-case (as indicated by Ptot).

The very best which can be achieved with direct mounting of TO-220 case is about 0.8°C/W with thermal grease. When an isolation layer is used between the package and heatsink the thermal resistance will depend on the desired insulation properties; for mica thickness of 50 to 100 micrometers the thermal resistance case to heatsink is about 1.5 to 2.3°C/W [2]. For other cases, the case-heatsink thermal resistance was considered to be proportional with the case area Ac. The results for different transistor cases are presented in table 1.

Table 1

| Т | Ac | | Thermal | Resistance | ΔT | Pd | Ptot | Dtot/Dd | | | |
|--------------------|---------|-----------------|---------|------------|------|------|------|---------|------|------|--|
| case | example | mm ² | j-c | c-hs | hs-a | j-a | °C | W | W | W | |
| TO-3 | 2N3055 | 600 | 1.5 | 0.20.7 | 1.53 | 3.55 | 150 | 4530 | 115 | 2.54 | |
| TO-218 | SGSD100 | 300 | 1 | 0.41 | 1.53 | 35 | 100 | 3320 | 130 | 46.5 | |
| ТО-220 | BD709 | 150 | 1.7 | 0.81.5 | 1.53 | 46 | 100 | 2517 | 75 | 34.5 | |
| | BDW93 | 150 | 1.6 | 0.81.5 | 1.53 | 46 | 100 | 2517 | 80 | 34.5 | |
| TO-126 (SOT-32) | BD679 | | 3.1 | | 1.54 | 610 | | 1710 | 40 | 2.54 | |
| | BD237 | 75 | 5 | 1.53 | | 812 | 100 | 128 | 25 | 23 | |
| | BD139 | | 10 | | | 1217 | | 86 | 12.5 | 1.52 | |

The normal font size values in the table were considered for (usual conditions):

- an isolation thickness of about 50 micrometers,
- a heatsink made with a 3mm thick 120x120mm² square aluminium sheet (that has around 3°C/W [3]) and
- the maximum ambient temperature Ta=50°C.

The other values: the transistor case area Ac, the junction-case thermal resistance R_{th} -c-a, the maximum junction temperature Tj (that determines the maximum temperature variation ΔT) and the maximum allowable power dissipation P_{tot} were estimated from the transistors data-sheets.

Using table 1, one can extract a rule of thumb: for usual conditions, the maximum power dissipation for a power transistor can be considered to be 1/4 of P_{tot}.

2.3 Choosing the final transistors in practice

Some simple relationship must be found considering the most important elements only (a first approximation analysis of the final stage). The usual relationships connecting some circuit elements and electrical quantities are:

$$\frac{R_E}{R_L} = \frac{1}{10}, \qquad \frac{R7}{R6} = 2, \qquad \frac{V_{op}}{V_{CC}/2} = k_{vn} = 0.8$$
 (5)

where k_{vn} is the voltage supply utilizing coefficient considered for nominal output power P_{on} (theoretically, the maximum k_{vn} is 1)

The relationship between the nominal output power and the maximum transistor power dissipation can be found from (1) and (2), for typical k_{vn} :

$$P_{dF\max} \cong 0.2P_{o\max} = 0.2\frac{P_{on}}{k_{vn}^2} \cong 0.31P_{on}$$
 (6)

The power transistors in the final stage can be selected based on (6) and Table 1. The results are presented in the last columns of table 3.

In order to keep the efficiency of the circuit high and to avoid the utilizing of a heatsink for the pilot transistor, two supplimentary conditions regarding the power dissipation in Q2, must be considered:

 $P_{D2} \le 0.1 P_{un}$ (for $P_{un} < 10$ W) and $P_{D2} \le 1$ W (for a BD139 as Q2). (7)

For a two-transistor structure of the final stage (without Darlington), the current gain of the transistors is also an important parameter. Considering the equivalent circuit of the final stage presented in figure 3 (for the nominal peak output voltage V_{op}), one can find the condition concerning the Q4 current gain (β 4= β F). The instantaneus voltage in (A) and (B), for the values given in (5) (and for $V_{BE} \cong 0$), are:

$$V_{A\max} = V_A + V_{op} = \frac{5V_{CC}}{6} + k_{vm}\frac{V_{CC}}{2} = 1.23V_{CC},$$
(8)

$$V_{B\max} = V_{op} \frac{R_{L} + R_{E}}{R_{L}} + V_{C5} = \frac{V_{CC}}{2} \left(k_{vn} \frac{R_{L} + R_{E}}{R_{L}} + 1 \right) = 0.94 V_{CC}.$$
(9)

The maximum input current in the final stage, and maximum R7 are:

$$I_{iF\max} = \frac{k_{un}V_{CC}}{2R_{L}\beta_{F}}, \quad R_{7} \le \frac{V_{A\max} - V_{B\max}}{I_{iF\max}} = \frac{0.29V_{CC}}{k_{vn}V_{CC}}2R_{L}\beta_{F} = 0.72R_{L}\beta_{F}.$$
(10)

From (7) and (10), the minimum β F can be found:

$$P_{D2} = \frac{V_{CC}}{2} I_{C2} = \frac{V_{CC}}{2} \frac{V_{CC}}{2 \cdot 1.5 \cdot \text{R7}} = \frac{V_{CC}^2}{2 \cdot 3 \cdot 0.72 \beta_F R_L} = \frac{P_{on}}{0.346 \beta_F} \le 1 \text{W}, \quad (11)$$

$$\beta_F \ge 2.9 P_{on} \quad (\text{with } P_{on} \text{ given in W}). \quad (12)$$

This is the minimum theoretical value. Practically, a current should flow in Q2 in any case. Greater the current variations in Q2, greeater the voltage variations (at the pilot input) and greater the THD factor. A minimum current in Q2 (for the nominal output voltage peak V_{op}) greater than $0.5I_{iFmax}$ will be considered. The quiescent current in Q2 (and in R7) should be increased $(I_{R7} \ge 1.5I_{iFmax})$ by decreasing R7 (and R6) correspondingly. The equation (12) becomes:

 $\beta_{\rm F} \ge 2.9 \cdot 1.5 P_{on}$ or $\beta_{\rm F} \ge 4.4 P_{on}$ (with P_{on} given in W). (13) In table 2 the cases when the two-transistor structure can be used are presented.

Table 2

| Line | P_{on} (W) | $I_{op}\left(\mathbf{A}\right)$ | βF | BD237 | BD709 | Selected |
|------|--------------|---------------------------------|-----|---------|---------|----------|
| 1 | ≤10 | ≤1.42.6 | ≥44 | Ic≤1.5A | Ic≤4.5A | BD237 |
| 2 | 15 | 1.73.2A | ≥66 | Ic≤1.1A | Ic≤3.2A | BD707 |
| 3 | 20 | 23.7A | ≥88 | - | Ic≤2.2A | - |

The collector current at whom the transistor has the given current factor is taken from the transistor data-sheets. The algorithm for selection the final transistors in all the possible cases (all the projects) is presented in table 3. In the last case (code T3) the Darlington structures should be made utilizing discrete components.

Table 3

| Condition | | Ic≤1.5(A) | $P_{on} \leq 15$ | $P_{dF} \le 10$ | $P_{dF} \le 17$ | The rest, $P_{on} \leq 100 \text{ (W)}$ | | | |
|-----------|----|-----------|------------------|------------------|------------------|---|-------|--|--|
| Туре | Q4 | BD237 | BD707 | BD679 | BDW93 | BD183 | BD139 | | |
| | Q5 | BD238 | BD708 | BD680 | BDW94 | (2N3055) | BD140 | | |
| Code | | S2 | T2 | S6 | T2W | T3 | | | |
| Notes | | | | $P_{on} \leq 30$ | $P_{on} \leq 55$ | $PdF \leq 30 (W)$ | | | |

| - | B | I | U | ≣ | ≣ ∃ | • • • | 9 | %, | ◆ 0 00 00 ◆ 0 | 3 🚅 | • | • | े 🙆 🖥 | - 🔺 - | | | | |
|-----|---|----|----|----|-------|-------|----------|------|------------------|-------|------|-----|-------|-------|---------|----|------|------|
| = | = =IF(PdF>17;"T3";IF(PdF>10;"T2W";IF(Pon>15;"S6";IF(lop>1.5;"T2";"S2")))) | | | | | | | | | | | | | | | | | |
| Ε | F | G | Н | J | L | 0 | Р | R | Т | U | X | Y | Z | AB | AC | AD | AG | AH T |
| Por | i RL | f١ | fh | Та | Vop | Vcc | Kvn | Iop | PdF | Ptot | TpTz | Cfg | Cfg1 | βFvf | IiFM(m) | KR | ∨вм | |
| 8 | 8 | 20 | 20 | 35 | 11.31 | 28 | 0.81 | 1.41 | 2.48 | 6.2 | S2 | 1 | 0 | 49 | 28.57 | 2 | 27.1 | 34.8 |
| 10 | 4 | 25 | 15 | 45 | 8.94 | 22 | 0.81 | 2.24 | 3.06 | 7.7 | T2 . | 1 | 0 | 89 | 25.00 | 2 | 21.5 | 27.5 |
| 70 | 3 | 30 | 12 | 35 | 20.49 | 52 | 0.79 | 6.83 | 22.83 | 57.1 | T3 | 2 | 0 | 1757 | 3.89 | 2 | 49.9 | 64.2 |
| 20 | 8 | 15 | 25 | 60 | 17.89 | 44 | 0.81 | 2.24 | 6.13 | 15.3 | S6 | 2 | 1 | 5000 | 0.45 | 2 | 43.1 | 55.0 |
| 35 | 4 | 25 | 15 | 45 | 16.73 | 42 | 0.80 | 4.18 | 11.17 | 27.9 | T2W | 2 | 1 | 3653 | 1.15 | 2 | 40.8 | 52.1 |

Figure 4.

In figure 4 the Excel function utilized to select the final transistors can be seen.

3. THE POWER TRANSISTOR MODELS IN EXCEL

To choose the other elements of the circuit, the electrical quantities should be computed and the transistors should be replace by simple models. The simplified transistor model can be used if the current domain does not include the high and the low current domain, but this is not the case for the transistors in the final stage.

The current factor of the power transistors is proportional with 1/Ic in the high current domain [1]. The linear approximation is more convenient for the Darlington transistor (the model is different compared with a normal transistor because of the internal resistors connected inside the Darlington package). Figure 4 and Figure 5 presents the models (with dash line) and the data-sheet curve β =f(Ic) (with normal line) for the BD707 and for the BDW93 transistor. For the examples in figures, the model functions are computed considering two points on the data-sheet curve:

$$\beta_{\text{BD707}} = \frac{200}{I_C}$$
 and $\beta_{\text{BDW93}} = 5200 - 600 I_C$. (14)

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Ic(A) 0.01 0.1 0.5 1 1.5 2 3 4 5 5.5 BD707 200 250 220 160 125 100 72 52 40 33 aprox_1/x 200 200 200 200 133.3 100 66.7 50 40 36.4



Ic(A) 0.5 1 2 3 4 5 6 7 BDW93 3000 4000 4300 3700 2900 2200 1700 1300 aprox lin 4000 4000 4000 3400 2800 2200 1600 1000



Figure 4.

Figure 5.

Based on the transistor models, the circuit elements for each project were computed on one line of the first Excel worksheet, so that the projects can be compared. Some amplifier parameters: the voltage gain, the input and the output resistance, are computed. In the second workbook, for one project (selected by its first workbook number) the harmonic distortion factors are computed. Some checkpoints are inserted (such is the minimum voltage in Q2 collector). Every element can be redefined and the parameters of the amplifier are re-computes. The tutor can test the student's ideas and verify the effects on the amplifier parameters.

4. CONCLUSIONS

This paper presents a systematic procedure for choosing power transistors, starting from the theoretical conditions, analyzing the maximum power dissipation of transistors in real conditions for different cases, and indicating the practical method that can be applied in any application. The case of Bootstrap configuration was specially. The algorithm of selecting the transistors and the implementation in Excel are presented. In the second part of the paper the power transistors and Darlington models (that can be used in Excel) are proposed and verified.

The tutors can use the analysis presented in this paper to verify the student individual projects and to provide the top students with the basic knowledge about the expert systems. The results given by the design method presented in this paper proves itself correct and useful during the last three years when the authors utilize it in Transilvania University of Braşov.

5. REFERENCES

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