TOWARDS SYSTEM-ON-A-CHIP DESIGN OF HIGH-SPEED DATA ACQUISITION SYSTEMS

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Abstract - **The present paper is aimed at proving the feasibility of system-on-a-chip (SoC) implementation of high-speed data acquisition system (DAS). Such a system consists of a very fast parallel analog-to-digital converter (ADC) and memory. The work and related investigations rely on top-down methodology – from system requirements to component specifications and design– taking into account sampling rate, power dissipation, die area and noise.**

Index Terms - **System-on-a-Chip, High-Speed Data Acquisition System, Parallel Analog-to-Digital Converter, Memory, Design and Test.**

"The principal applications of any sufficiently new and innovative technology always have been and will continue to be applications created by that new technology"
"The Futility of Predicting Applications"
Herbert Kroemer, 2000 Nobel laureate[1]

I. INTRODUCTION

The demand of large systems integrated on a single chip increased substantially in recent years. The classic ASIC technology evolved to System-on-a-Chip (SoC) technology, becoming now widespread. There are a few major reasons for presenting this paper. The first one:
"We define an System-on-a-Chip as an IC, designed by *stitching together multiple stand-alone VLSI designs to provide full functionality for an application"*[2].

In other words, SoC is a concept that integrates pre-designed, reusable components, so called Intellectual Property (IP) cores. At first glance, though there are some hidden hurdles, the pure digital SoC seems facile and – as a joke – could be named "Mouse Aided Design". But analog, RF and mixed signal cores still are not easy portable and could cause a wide range of problems in terms of compatibility, power consumption, noise emissions and immunity, area etc. The general today's tendency is to use digital CMOS process for all IC products, including – certainly - mixed signal circuits. But this process is optimized mainly for the trade-off between speed, power and area. Razavi [3] points out that analog circuits entail a multidimensional design space and offers an octagon where every two parameters trade with each other.

Another major reason for this paper is the importance of the right choice of the system to be implemented as a SoC, as well as estimation of the feasibility of the whole project. In search for such a system in this paper is proposed a conventional

high-speed data acquisition system (DAS) consisting of a parallel analog-to-digital converter (ADC) and memory (Fig.1). It is attractive because of the very small

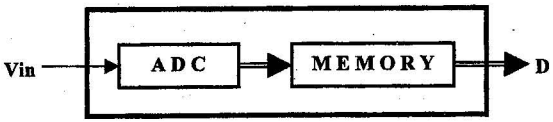

Fig.1. High-speed data acquisition system.

number of pins and relatively small analog part (a set of ADC's identical comparators) versus the large maximum possible memory. In this thread of thoughts it is worth noting: i) the author's idea for high-speed DAS implementation on a single chip, dated as far back as 1992 [4]; ii) the project of LeCroy "Multichip Module - 8bit ADC and 4MB memory"[5], which is a step to a whole digitizer-on-a-chip.

The content of this paper is organized as follows. In Section II are discussed some general considerations. Next three sections are devoted to the analog-to-digital converter, memory and test. Concluding remarks are in Section VI.

II. DESIGN CONSIDERATIONS

The modern very fast DAS meet the needs for high conversion rate of analog signals in wide area of digital signal processing (DSP) in instrumentation, communications, military applications, scientific researches etc. In Fig.2 is depicted a top-down approach to the design of high-speed DAS, firstly proposed in [6] and developed in this paper. It starts with various applications – digital storage oscilloscopes, logic analyzers, video and multimedia, radars, lasers, high-energy physics etc. A common identical part of all applications is the high-speed DAS. It is followed by specific for each application DSP, which should be integrated in near future with DAS.

The purpose of this work is to specify and provide a few insights into the design of system components – the shaded blocks in Fig. 2 – as well as to propose some new ideas concerning their behavior and schematics. The main parameters under consideration and the interaction between them are presented in the hexagon of Fig.3, according to the upper mentioned idea of Razavi [3].

III. ANALOG-TO-DIGITAL CONVERTER

The "heart" of a DAS is the high – speed ADC. Over last decade the power consumption of the most commonly used parallel synchronous (flash) ADC has been reduced from 5W to 20-30 mW, thanks to new architectures – pipelined, folded, two- and multistep [Fig.1] and related circuit techniques based mainly on CMOS technology. At the same time there has been a revival of asynchronous design methods. In light of this, the asynchronous parallel ADC (Fig.4) proposed in [7]

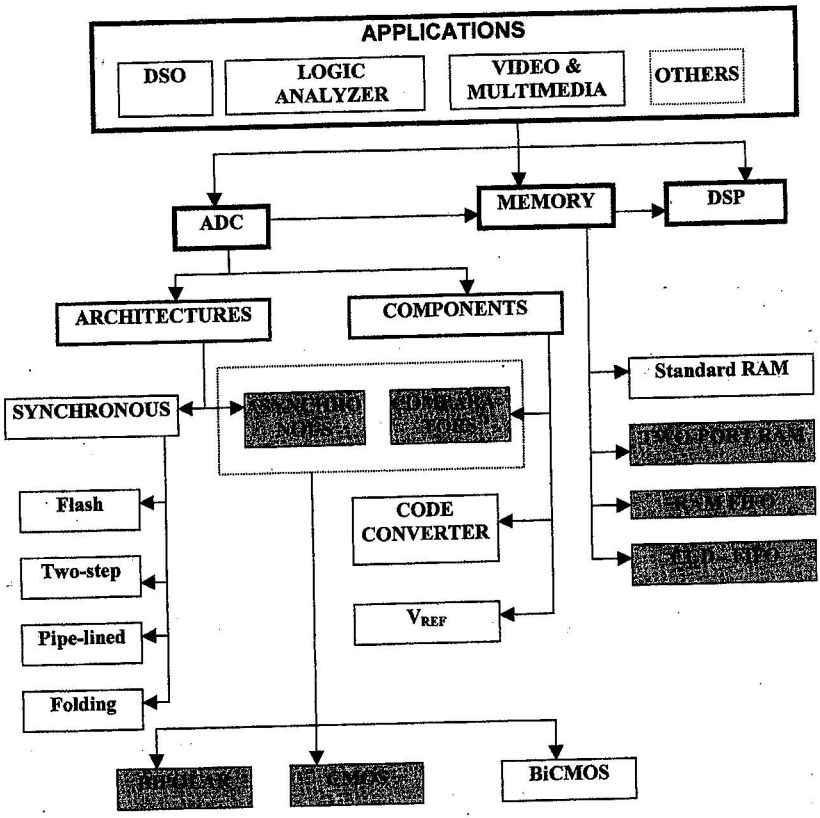

Fig.2. Top-down methodology.

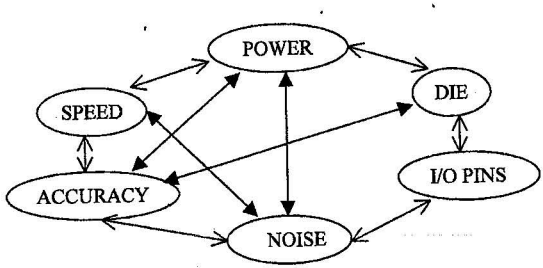

Fig.3. Parameters and design trade-off.

differs from its synchronous counterpart by absence of any clock signal, except the output register. The moment of every comparator switching is determined by the input signal itself, like a tracking ADC. This mode of operation has some advantages in terms of power saving and reduced noises. They can be proven briefly as follows.

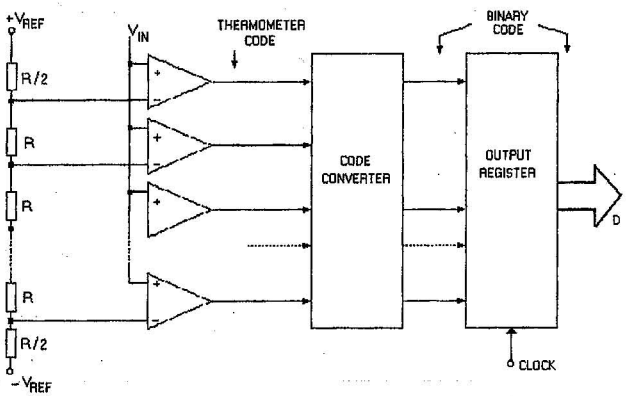

Fig.4. Block diagram of an asynchronous parallel ADC.

The power consumption of a n-bit flash ADC during a clock signal is given by

(1) $P = 2^n Po,$

where Po is dynamic power consumption of a single comparator. The Nyquist theorem requires the signal sampling to be performed at least twice within one period. Thus the total power consumption during thje whole signal period is

(2) $P_T = 2^{n+1} Po$

In practice, however, since no signal is truly bandlimited, in order to avoid alias phenomena, sampling is performed 5-10 times within the signal period and the total power consumption is augmented to

(3) $P_T = c\ 2^n Po,$

where c=5-10 instead 2.

In order to calculate P_T of the asynchronous ADC, let consider an input signal changing over full scale range within the frames of one period, e.g. sinusoid. Since every comparator switches two times, then all 2^n comparators consume total power

(4) $P_T = 2^{n+1} Po$

This is the same result as (2), but the power consumption of an asynchronous parallel ADC is distributed over the whole signal period (more or less uniformly, depending on the signal waveform), instead of being "flashed" only in the moments of clock sampling. Hence the asynchronous behavior reduces to a considerable extent (up to 2^n times) the noises through common substrate, supply lines and electromagnetic emissions. Moreover, in real applications the total power consumption should be lowered by a factor of c/2 = 2.5 - 5.

Key – components of the parallel ADC are the comparators. In order to meet specific needs of the asynchronous ADC, some original schematics have been proposed and investigated for bipolar [8] and CMOS [9,10] technologies. The circuit design is based on the use of so-called "dynamic hysteresis"[8]. The comparators feature one threshold, fast switching rate with positive feedback and controllable short-time noise immunity just after threshold crossing. The last one makes them very suitable for asynchronous applications.

IV. MEMORY

Among the possible different kind of memories – candidates for our task, shown in Fig.2, the shaded ones are suitable. The most attractive is FIFO built by dynamic shift registers, especially in CCD design style and technology. This memory has advantages with respect to power consumption/dissipation, area, speed and simple synchronization of data transfer from ADC and to the computer (provided that the bus and computer are able to accept so fast data stream). As for data transfer, two-port RAM and RAM-FIFO have better performance.

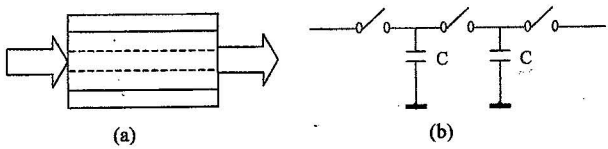

Fig.5. (a) Register FIFO memory. (b) CCD cell

POWER DISSIPATION. The memory capacity to be implemented in SoC is limited mainly by the power dissipation. That's why it should be very useful for different kind of memory to obtain the relation of power dissipation P with respect to memory capacity N and working frequency F. By way of example let consider a CCD-FIFO (fig. 5) based on a two pass-gate cell. If $P_G = p\ \mu W/MHz$ is specific power for one gate, then the total power dissipation of the memory equals

(5) $$P_W = 2\, p_{\mu W} \cdot N_{Mbit} \cdot F_{MHz}$$

This relation is drawn in Fig.6 for different memory size and p = 0.005. Taking into account, as mentioned previously, ADC's power is relatively small, it could be neglected. Then from Fig.6 is evident how the power constraint, imposed by the package, and working frequency determine the memory capacity. For instance, a 10 bit 100 MHz ADC can be integrated with a memory of 100K words without exceeding 1W maximum power dissipation.

This result will be different for another kind of memory, due to its internal structure. There should be taken into account specific memory characteristics, e.g. average cell switching activity, bit-line power consumption etc.

DATA TRANSFER. The addressing capability of static RAM-based memories (two-port RAM and FIFO-RAM) is a specific favorable feature, which suggests a

sophisticated data transfer, aimed at more efficient use of the on-chip-memory. Let consider next example. The sampling rate of most up-to-date parallel ADC is within the range of 100-1000MHz. Hence, this is the frequency F_{WR} of write memory operation. The frequency of read operation F_R is limited by the bus throughput, e.g. 400MHz for a 2.4GHz Pentium based computer.

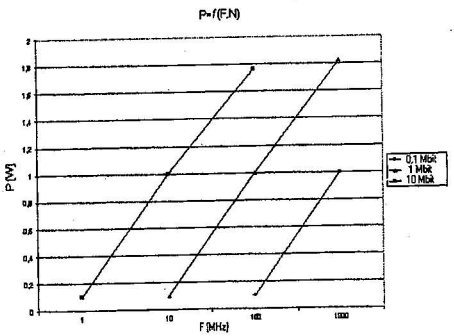

Fig. 6. Power dissipation of a CCD-FIFO memory

Thus, $F_{WR} > F_R$, but both frequencies are of the same order, i.e. $\frac{F_{WR}}{F_R} = m = 2,3,4$ etc. If read and write operations are performed simultaneously, then from ADC's point of view, the real memory size M_{REAL} seems like a bigger virtual memory M_{VIRT}. It is easy to prove the relationship

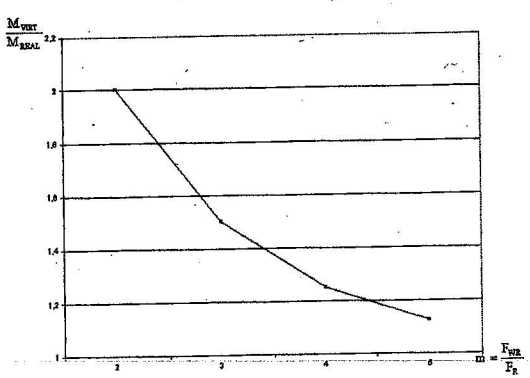

Fig.7. Virtual versus real memory.

(6) $$\frac{M_{VIRT}}{M_{REAL}} = \frac{m}{m-1}$$

illustrated in Fig.7. For instance for m=2, the memory space for ADC data is 2X versus the physical one.

V. TEST

Specific features of the present system blocks – very high speed operation and large memory – suggest on–line testing. For that purpose is proposed the architecture shown in Fig.8. It relies on the use of an additional internal bidirectional bus and local block buffers B. Three new pins – C_0, C_1 and external clock – select and enable exhaustive test of the ADC and standard functional test of the memory. The only area overhead is due to the buffers' control logic and internal bus.

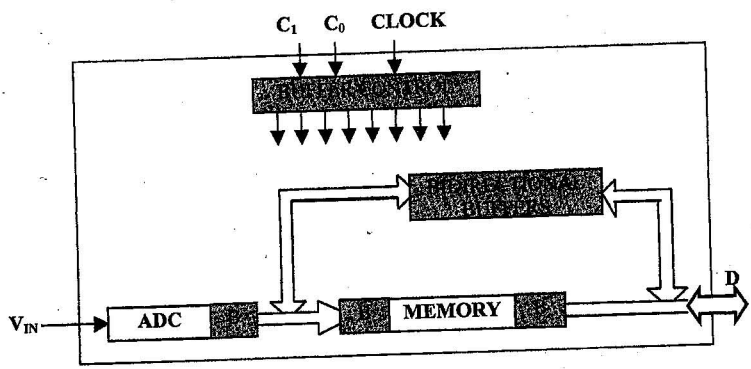

Fig. 8. On – line testing of the SoC blocks - ADC and memory.

VI. CONCLUSIONS

The main results of the investigations aimed at system-on-a-chip implementation of high-speed data acquisition system are as follows:

- An asynchronous mode of operation of the parallel ADC is proposed. It has advantage in terms of power saving and noise immunity in comparison with the most commonly used parallel synchronous (flash) ADC. Comparator circuits tailored for asynchronous ADC, i.e. working without a sampling clock, are developed and reported in previous author's papers;
- An approach for determining memory capacity is proposed. It consists in obtaining an analytical expression of power dissipation with respect to memory capacity and working frequency. By this means is possible to keep power constraint at maximal rate and memory size. An example related to CCD–FIFO memory is given;

- It is proven that RAM–based FIFO memory is very convenient for data transfer to the computer, for allows efficient use of the memory space when the sampling frequency of ADC is commensurable to the transfer rate, as is often the case;
- A circuit for on–line test of the ADC and memory is proposed. It requires very small area overhead and only three additional pins.

Analytical and simulation results proving the feasibility of SoC design and implementation of a high-speed data acquisition system are reported.

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