MODELING AND INVESTIGATION OF THE CHARACTERISTICS OF SUCCESSIVE APPROXIMATION REGISTER

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The problem that was set is to create a model of successive approximation register (SAR) for well-known simulation program OrCAD PSpice. It is implemented an original idea, which consists of building the register with shift register with initially loaded logical 1 (other outputs are 0) and sequentially enabling of trigger cells, which save the current information coming from the comparator and thus forming the output code. Two internal architectures of the model of SAR were developed. The first one is built on trigger cells that are latch type and the other – on flip-flops. For comparing the results is developed a third modification of the model, based on a known scheme solution with ordinary register. The investigations emphasize on accuracy as well as a speed of conversion.

INTRODUCTION: The design of new data acquisition systems and devices is inconceivable without data converters (analog-to-digital and digital-to-analog-converters) [2-4]. This necessitates the need of developing of models of such devices. One of the most widespread kind of analog-to-digital converters (ADC) is the successive approximation ADC and the reason of this is that it comprises two very important features: comparatively high conversion time with simple structure. The main component in building the successive approximation ADC is successive approximation register (SAR). The aim of this work is to present the new scheme solution in modeling the SAR as well as to give some results of simulations of variants of ADC, using the model of SAR.

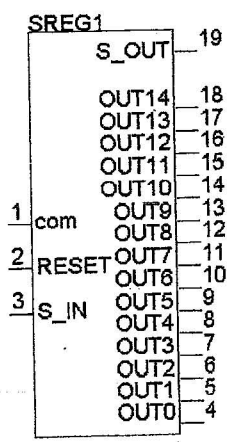

fig.1. A symbol of SAR

MODELING AND SIMULATION: The appearance of the model of SAR in PSpice simulation program is shown in fig.1. The symbol is for 15 bit register. The destination of the pins is the following: 1 – **com** is the input that is tied to the output of the comparator; 2 – **RESET** is used for clearing the internal shift register and trigger cells and then setting the initial

1 in the shift register; 3 – **S_IN** is connected to clock generator; 4-18 are the outputs of the successive approximation register and 19 – **S_OUT** is used for initial settling of the other schemes connected to the register if it is needed (for example, by connecting CDAC).

The internal structure of the SAR, using latch triggers is given below (fig.2). When the signal to RESET is logical zero, all components are cleared, except the

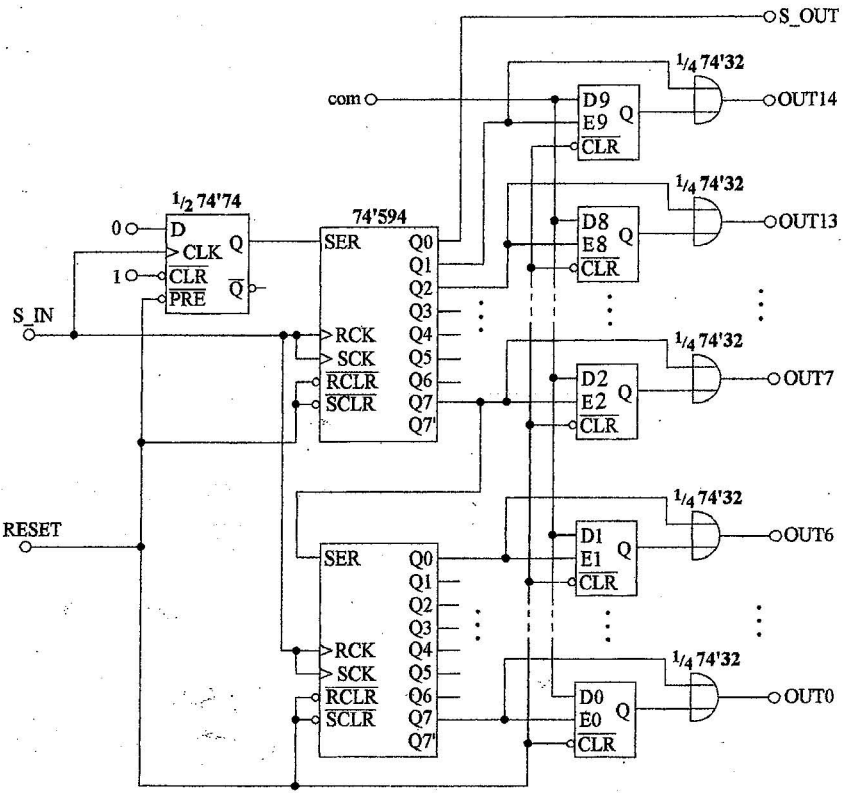

fig.2. Internal structure of SAR with latch triggers

trigger 74'74, whose output is high. The change of the state becomes if RESET is high and if there is a rising edge on S_IN pin. In this very moment the shift register 74'594 accepts the logical one settled to its serial input SER, and the IC 74'74 accepts the logical zero to from its data input. By the next rising edge of the clock on the output Q0 of the shift register appears the logical one. This indicates the initial state to the other devices connected to the successive approximation register. The third rising edge on S_IN after RESET state, the logical one form output Q1 is shifted

to the output Q2 of 74'594. Thus begins the substantial part of the conversion process. The logical one comes to the output OUT14 through OR gate. On that way the SAR provides such code to DAC that it gives an analog voltage that is a half of the full scale voltage. The response of the comparator shows if the logical one remains or not. The output of the comparator is high if the value of the measured voltage is between half and full scale voltage. Exactly this state of the comparator is saved to the single enabled in that moment latch trigger. By shifting the logical one to less significant bits, gradually is formed the output code corresponding with the measured voltage, that continuously is compared with output voltage of DAC.

By means of table 1 could be comprehended the conversion process. It is shown the action of 14 bit successive approximation register by the concrete value of the measured voltage U_x and the reference voltage of DAC U_{ref}.

Table 1

U_{ref}=5,12V; U_x=2,7535V				
	Code to DAC	U_{DAC}, V	U_{com}, V	The state of the trigger in the corresponding bit
RESET=0	00000000000000	0	5	-
I cycle	10000000000000	2,56	5	1
II cycle	11000000000000	3,84	0	0
III cycle	10100000000000	3,20	0	0
IV cycle	10010000000000	2,88	0	0
V cycle	10001000000000	2,72	5	1
VI cycle	10001100000000	2,80	0	0
VII cycle	10001010000000	2,76	0	0
VIII cycle	10001001000000	2,74	5	1
IX cycle	10001001100000	2,75	5	1
X cycle	10001001110000	2,755	0	0
XI cycle	10100001101000	2,7525	5	1
XII cycle	10010001101100	2,75375	0	0
XIII cycle	10001001101010	2,753125	5	1
XIV cycle	10001001101011	2,7534375	5	1
	10001001101011			

The last row of the table presents the final code of SAR.

The internal structure of SAR with flip-flop triggers is shown in fig.3. The difference here is that the trigger is enabled only by the falling edge of the clock signal S_IN and, of course, EX must be one in that moment. EX is the corresponding output of shift register.

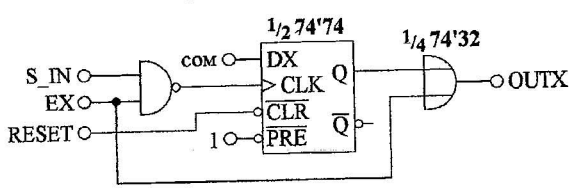

fig.3. Internal structure with flip-flop triggers

Another simulated

internal structure, that is already known [2], is presented in fig.4. Here is applied an ordinary flip-flop register 74'273.

The simulation is not running if there is no NAND and NOT gates, though, at first glance, it is the same to connect the com and S_IN to the inputs of AND gate. Another special feature by using of flip-flop register is the feedbacks from the outputs of SAR to the data inputs of the register '273.

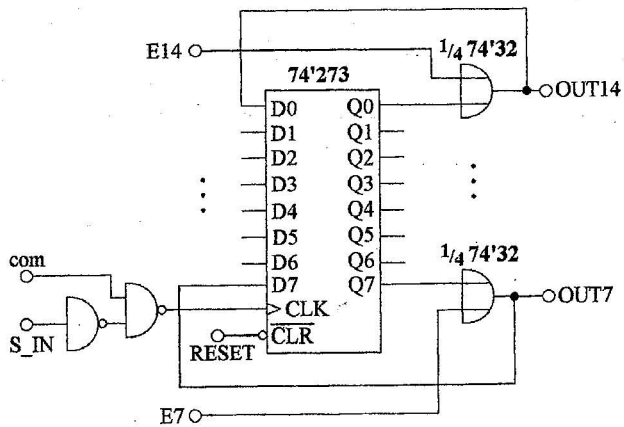

fig.4. Internal structure of SAR with ordinary register

The simulated scheme of successive approximation register with ordinary DAC in the PSpice environment is given in fig.5.

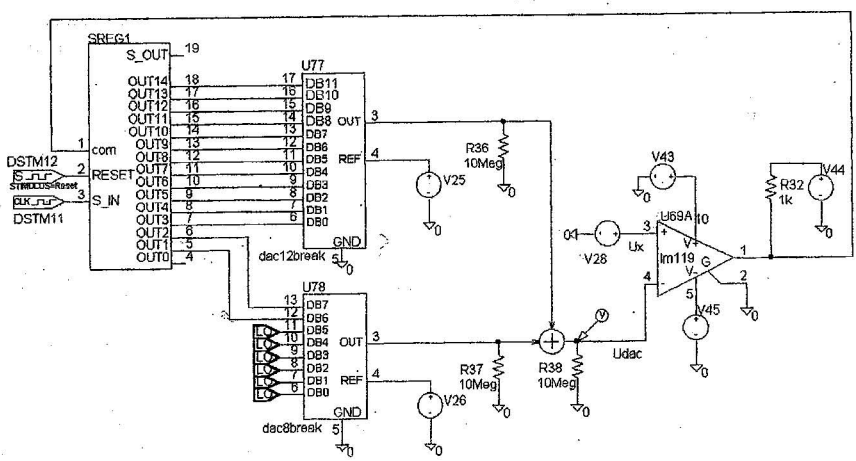

fig.5. A simulated scheme of 14 bit ADC with SAR, using ordinary DAC

In PSpice program there is ideal models only for 8, 10 and 12 bit DAC. The shown connection of one 12 bit and one 8 bit DAC with a summing circuit implements the action of 14 bit DAC. The reference voltage of the 8 bit DAC is equal to the quant of 12 bit DAC. LM119 is a high speed comparator with TTL output

levels. The simulation results by realizing the three different, mentioned above, architectures of SAR show that SAR with latch trigger cells and flip-flops give almost similar time of conversion and SAR with ordinary register nearly 2 times longer time of conversion.

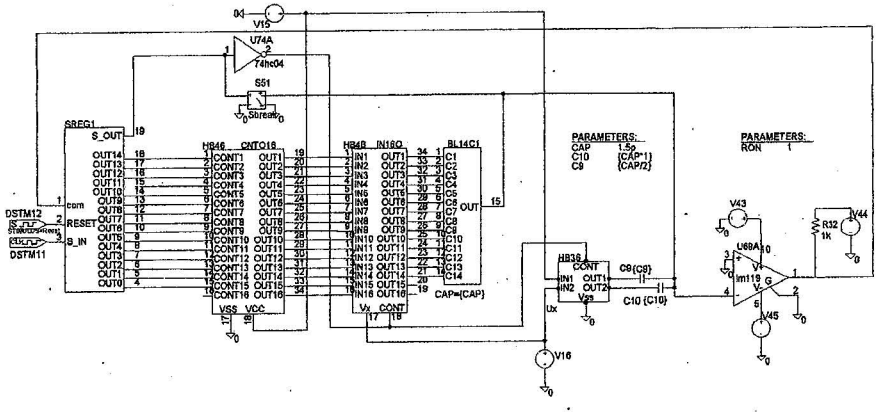

fig.6. A simulated scheme of 14 bit ADC with SAR, using capacitor DAC

A second simulated scheme, using the developed model of SAR is shown in fig.6. It is the ADC with capacitor DAC[1;3]. The block components CNTO16 and IN16O carry out the needed connections by every step of the conversion process to the block of capacitors BL14C1. The values of the capacitors and turn on resistance of the switches are parameterized.

In order to be followed the conversion process is written the function in MATLAB, that computes the voltages to inverting input of the comparator. The description of that function is the following:

[code,uk]=sregcap(c,uref,ux,n).

As it can be seen, besides the voltages to inverting input of the comparator, involved in vector **uk**, there is also another output vector of the function and it is the output code (**code**). The inputs are value of basic capacitor **c**, the value of the reference voltage **uref**, the measured voltage **ux** and number of bits of ADC **n**. This function computes only steady mode of the steps in conversion process, i.e. these are ideal voltages that could be set in the end of transient mode by every change of the code. The simulations in PSpice show that there are little differences between real obtained voltages **ux** and computed in MATLAB. The non-ideal parameters of the comparator are also the reason for the differences. The investigations show that by excluding the comparator influence the output code depends on frequency of the clock and the time constant (the product R.C, where R is the turn on resistance of the switches). The results in different cases confirm the fact that despite the differential

equation system is too sophisticated, the time response could be approximated by one exponential expression. Then the problem is reduced to find the needed time the voltage of the capacitor of one RC group to reach the normed value 1 minus relative error. The account is the following:

$$1-er=1-e^{-\frac{t}{\tau}}\ ;\ er=e^{-\frac{t}{\tau}};\quad \ln(er)=-\frac{t}{\tau};\ t=-\ln(er).\tau .$$

Since the time constant for the largest capacitor is τ=RC.2^{n-1} and the required error is $½^n$, for n=14; R=1Ω and C=3pF, t is obtained 238,5 ns. The simulation results really show that the clock period must be greater than 220 ns in order to be the output code correct.

CONCLUSIONS: Computer model of a successive approximation register with different architectures to general purpose analysis program OrCAD PSpice is developed. An original idea of constructing the model is implemented. The models show a good functionality and allow investigation of the characteristics of analog-to-digital converters by means of this model of SAR. Successful simulation of ADC with ordinary DAC and capacitor DAC is accomplished. The simulation results by realizing an ADC with normal DAC show that by using SAR with latch triggers and flip-flops give almost similar time of conversion and by using SAR with ordinary register nearly 2 times longer time of conversion. The results of investigation of ADC with capacitor DAC show that it is needed time to overcharge the capacitors and this time could be estimated by values of turn on resistance of the switches, capacitance of the greatest capacitor and using the results of the transient process of ordinary RC circuit.

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