SYSTEM ON CHIP DESIGN – A REASON EU PROJECT

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Hristov M.H., System on Chip Design – A REASON EU Project. *The main goal of the REASON (Research and Training Actions for System on Chip Design) Project is to facilitate integration of the academic and research institutions of Central and Eastern Europe (CEE) working in the field of microelectronics into the mainstream R&D activities going on in the EU countries. To achieve this goal, the project aims at raising the level of education and research as well as the number of highly-skilled researchers and designers in the field of microelectronic design in CEE countries, in order to facilitate co-operation in research and development with European R&D institutions and industry, to reduce the microelectronic skills shortage in Europe and to minimise the consequences of this shortage.*

1. INTRODUCTION.

Microelectronics is nowadays and will remain in the foreseeable future the crucial enabling technology in the development of the information society and the strategic sector of the industry for maintaining the competitiveness of the European economy. As a result of rapid increase of the number and complexity of the microelectronic systems necessary for new innovative products, the demand for highly skilled microelectronic designers is quickly growing. Unfortunately, the supply of microelectronic designers and researchers is far below the demand. Critical shortage of electronic engineers skilled in design of microelectronic circuits and systems is observed all over Europe, and has become a concern of primary importance for the industry.

Despite difficulties, the countries of Central and Eastern Europe managed to maintain their intellectual potential in education and research in the field of microelectronic design. However, this potential is currently underutilised. To exploit this potential, the existing links with EU research institutions and industry must be strengthened and establishing of new links is highly desirable. Links of academic institutions with local enterprises should also be strengthened. To avoid excessive "brain draining", which can be damaging to education and local economies of Central and Eastern European countries, contacts with big European semiconductor manufacturers should go beyond mere "head hunting". Actions aimed at promotion of co-operation of the European industry with partners from Central/Eastern Europe will help to extend the European knowledge base and minimise the consequences of insufficient human potential in the field of microelectronic design.

The future of microelectronic design in Europe, including Central/Eastern Europe, depends also on the quantity and quality of candidates for related studies at universities.

Unfortunately, it is observed all over Europe that interest in science and technology among schoolchildren and high school students dropped dramatically. Careers in business, management, law etc. are considered more attractive. Therefore it is important to demonstrate to the European youth the beauty of engineering profession and in particular to raise interest in technical studies devoted to electronic engineering, including microelectronic design.

2. PROJECT OBJECTIVES.

Mission of the project. The main goal of this project is to facilitate integration of the academic and research institutions of Central and Eastern Europe (CEE) working in the field of microelectronics into the mainstream R&D activities going on in the EU countries. To achieve this goal, the project aims at raising the level of education and research as well as the number of highly-skilled researchers and designers in the field of microelectronic design in CEE countries, in order to facilitate co-operation in research and development with European R&D institutions and industry, to reduce the microelectronic skills shortage in Europe and to minimise the consequences of this shortage.

Objectives. For development of successful co-operation the following conditions must be met:

- The level of competencies and skills of researchers from Central/Eastern Europe must be high enough to allow participation in advanced and challenging research projects targeted at solving the problems faced by European electronic industry.
- State-of-the-art research infrastructure must be available and maintained in Central/Eastern Europe.
- The potential research partners from EU countries must be aware of competencies and achievements of their colleagues from Central/Eastern Europe.
- In the case of participation of SMEs, additional condition is their awareness of the IST programme and ability to absorb new technologies.

Therefore, the main objectives of the project are as follows.

(1) Raising the level of awareness of industrial problems and the level of competencies among researchers in Central/Eastern Europe in order to facilitate research co-operation with the European research institutions and industry. Special attention will be paid to methodologies of system-on-chip design and test (including low power VLSI circuits, design reuse and IP-based design) as well as methodologies of analogue and mixed signal IC design for wireless communication applications (such as RF CMOS circuits), networking, and multimedia.

(2) Strengthening of personal and institutional links between academic and industrial partners, both in EU countries and in the countries of Central/Eastern Europe, in order to facilitate formulation of new RTD projects and formation of project

consortia. These objectives can be achieved by training courses, „hands-on" training and workshops organised with participation of advisors and/or trainers from the industry, and from the academic and research institutions from EU member states which have experience in industrially oriented research or training and good links with the industry.

(3) Knowledge transfer to the SMEs in Central/Eastern Europe and raising the level of awareness of the IST programme, in order to facilitate participation of SMEs in RTD and other projects of FP5. This objective can be achieved by action aimed at identification of enterprises interested (at least potentially) in microelectronic design, by promotional and information actions, intensive courses and by distance learning, i.e. information and training materials available over Internet.

(4) Raising the interest in science and technology and in particular in microelectronics among high school students in order to ensure adequate supply of good candidates for university studies and in this way to maintain the social knowledge base in the field of microelectronics.

3. SYSTEM-ON-A-CHIP.

System-on-a-chip is an IC, designed by stitching together multiple stand-alone VLSI designs to provide full functionality for an application.

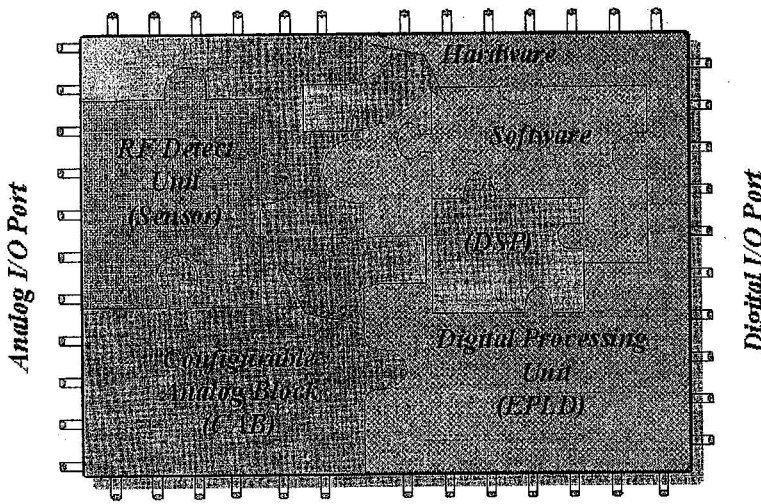

Fig. 1. Typical SoC

Looking at a typical SoC, shown in fig. 1 consists of several parts, known as cores

(terms such as intellectual property blocks, virtual components, macros, etc.) The cores must be adapted on each other exactly, like a Puzzle picture.

Because of the increasing integration of cores and the use of embedded software in SoC, the design complexity of SoC has increased dramatically and is expected to increase continuously at a very fast rate. Conceptually this trend is shown in the table below.

Future Projections for Silicon Technology						
Year of first DRAM shipment	**1997**	**1999**	**2003**	**2006**	**2009**	**2012**
Minimum Feature Size	250nm	180nm	130nm	100nm	70nm	50nm
DRAM Bits/Chip	256M	1G	4G	16G	64G	256G
DRAM Chip Size (mm^2)	280	400	560	790	1120	1580
Microprocessor Transistors/chip	11M	21M	76M	200M	520M	1.40B
Maximum Wiring Levels	6	6-7	7	7-8	8-9	9
Minimum Mask Count	22	22-24	24	24-26	26-28	28
Minimum Supply Voltage (volts)	1.8-2.5	1.5-1.8	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6

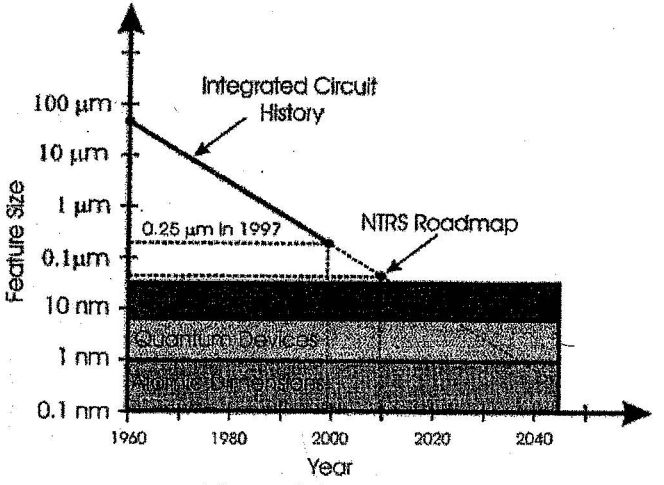

Fig. 2. Historical trends.

The development and/or the Design of such ASIC complicated SoC requires several process steps (fig. 3).

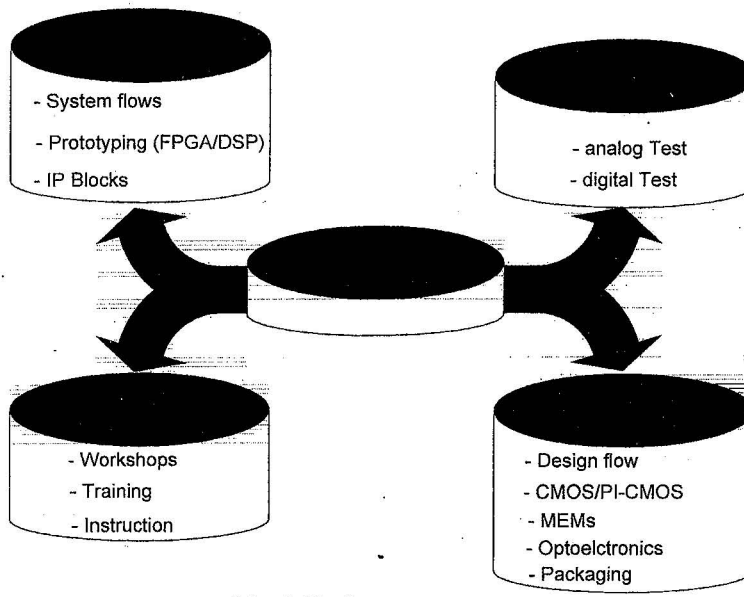

Fig. 3. Design process steps.

For each part there exist different methods and tools in the design process. Designers have to work together and find "common language". The main problems exist at the borders between the design worlds.

4. List of participants in the REASON project.

The project consortium includes 22 partners from EU member states and Central and Eastern Europe. The project is coordinated by Warsaw University of Technology, Warsaw, Poland. The EU partners will provide information, help and guidance for project partners aiming at joining EUROPRACTICE and start their training and research in close cooperation with the microelectronic community of the unified Europe.

The table below contains the names and countries of all participants.

Part. No.	Participant name	Participant short name	Country
1	Warsaw University of Technology	WUT	Poland
2	Institute of Electron Technology	IET	Poland
3	Tallinn Technical University	TTU	Estonia
4	Vladimir State Technical University	VSTU	Russia
5	Budapest University of Technology and Economy	BUTE	Hungary
6	Slovak University of Technology	FEI STU	Slovakia
7	"Politehnica" University of Bucharest	PUB	Romania
8	Ilmenau Technical University	TUI	Germany
9	Technical University of Lodz	TUL	Poland
10	Interuniversitair Micro-Electronica Centrum	IMEC	Belgium
11	Universite Joseph Fourier - Grenoble 1	UJF	France
12	Eindhoven University of Technology	TUE	Netherlands
13	Institute of Informatics of the Slovak Academy of Science	IISAS	Slovakia
14	Technical University of Sofia	TUS	Bulgaria
15	Lviv Polytechnic National University	LPU	Ukraine
16	Belorussian State University of Informatics and Radioelectronics	BSUIR	Belarus
17	Technical University of Liberec	TULC	Czech Republic
18	Kaunas University of Technology	KTU	Lithuania
19	Belarusian State University	BSU	Belarus
20	University of Ljubljana	UoL	Slovenia
21	Riga Technical University	RTU	Latvia
22	Rutherford Appleton Laboratory	CCLRC	UK

5. WORKPLAN.

The workplan includes the following activities:

- Introductory actions:
  - Analysis of needs of local industries in CEE countries,
  - Access to EUROPRACTICE by partners from Ukraine and Belarus.
- Training actions in the field of system-on-chip design and ASICs for wireless communication, networking, and multimedia.
- Practical training in usage and maintenance of advanced CAD tools.
- Development of EDUCHIP - special VLSI chip for microelectronic education.

- Topical workshops devoted to tutorial-based discussions of narrow but vital areas of research in microelectronic design.
- Development and deployment of Web-based training materials.
- Special conference sessions and/or tutorials on industrial and educational problems.
- Special promotional actions for high school students.
- Promotional actions associated with commercial events such as trade fairs.

6. WORKPACKAGES: AN OVERVIEW.

The project consists of 13 workpackages including a workpackage for project management. These workpackages cover all important areas of microelectronic design and microsystems.

Workpackage WP1: Introductory actions.

This workpackage includes actions preparing the partners for successful participation in other WPs.

Workpackage WP2: Methods and tools for System on Chip design

This workpackage consists of training actions and workshops devoted to the problems of SoC design, including such topics as hardware-software codesign and IP-based VLSI. Special attention will be paid to tools that are industry standard (such as the SYNOPSYS and CADENCE design toolsets and new SoC-oriented SystemC based tools) and are available to universities. This is one of the most important workpackages, with participation of almost all partners.

Workpackage WP3: Testing and design for testability of SoC

This workpackage is devoted to training in the field of test generation and design for testability of SoC. A specific feature of this WP is development of tools, objectives (generic project related tasks, also from industry) and innovative training methodology to carry out research training in the universities and for SME engineers to develop research skills and creativity in young engineers

Workpackage WP4: Analog and RF design

This workpackage consists of training actions and workshops focused on design problems and design tools for analog design and RF CMOS/BiCMOS/SiGe design, including wireless communication systems design. Modeling and simulation problems as well as low power analog design will also be included.

Workpackage WP5: Thermal modeling, simulation and testing

This workpackage will be devoted to thermal problems in microelectronic design. The main objective is to establish awareness of thermal problems among system level designers, since thermal problems are best treated at an early design phase.

Workpackage WP6: Microsystem design: methods and tools

This workpackage will consist of workshops and other training actions in the field of methodologies and tools for microsystem design, including micromechanical sensors

and actuators. The emphasis will be put on courses on current state-of-the-art and trends in microsystem design methodology and training on the available design tools. Physical and technological aspect of micro-(mechanical) sensors, actuators and other devices, their modeling and (on-)system simulation will also be included.

Workpackage WP7: Research training in new chip architectures

This workpackage aims at establishing an environment for training in design of microelectronic chips based on unconventional architectures such as reconfigurability based on genetic algorithms, artificial neural networks, fuzzy logic controllers, cellular automata.

Workpackage WP8: Technologies and contents for distance training

In this workpackage new Web-based training technologies as well as Web-based contents will be developed, exchanged and disseminated.

Workpackage WP9: The educational chip

The goal of this workpackage will be development, design, prototyping and manufacturing of EDUCHIP: an educational VLSI integrated circuit, to be used in student's labs in universities in the process of training in microelectronics and microelectronic design.

Workpackage WP10: Promotion and dissemination

This workpackage contains promotional and dissemination actions such as the annual MIXDES conference and other events open to everybody, not only to the project partners. Promotional actions addressed specifically to industry, in particular to SMEs, are also included.

Workpackage WP11: Actions addressed to high school students

This workpackage includes several types of actions aimed at raising interest in science and technology in general and in particular in microelectronics among high school students. Among these actions there are special lectures and presentations on microelectronics including interesting and futuristic applications, visits to clean rooms and lab facilities, development of Web-based multimedia material for schoolchildren.

Workpackage WP12: Future and emerging problems in microelectronics and microsystems.

This workpackage is reserved for actions that cannot be defined at the moment of the start of the project because they will result from further development of microelectronics and microsystems, new problems, new emerging design methods etc.

Workpackage WP13: Planning, management, assessment and evaluation

This workpackage contains all planning and coordination tasks.

7. Participation of Technical University of Sofia for the first project year.

WP1

- ***Task 1.1:*** Seminar "EUROPRACTICE – design, prototyping and education in Microelectronics".
  Two courses "Industry Standard Microelectronics CAD Software".

WP2

- ***Task 2.1:*** Seminar "Quality Problems in VLSI Design".
- ***Task 2.2:*** A summer course devoted to Methods and tools for System on Chip Design.

WP3

- ***Task 3:*** A workshop entitled "Testing and Design for Testability of Digital Circuits".
  A one-day tutorial.

WP4

- ***Task 4.1:*** Annual training course "Specific problems of manufacturability-oriented design of analog integrated circuits and device modeling".
- ***Task 4.2 (f):*** A lecture on "Physical and Technological Simulation and Design Application of submicron BiCMOS VLSI".

WP10

Organisation of an international conference "Electronics" 2002.

WP13

- ***Task 13.2:*** Technical/scientific management, assessment and evaluation.

8. Conclusion.

As a result of the completion of this project it is expected that research staff from more than 30 institutions in Central and Eastern Europe will be trained, at least 4 new EUROPRACTICE members will be enrolled, new courses will be developed and included in the EUROTRAINING portfolio, training and promotional actions targeted at SMEs (more than 500 existing in NAS countries and many more in Russia, Ukraine, Belarus) will be organised, new distance learning materials will be available on the Web, educational VLSI chip will be designed, prototyped and made available to European universities.