

# VIRIABILITY ANALYSIS OF ANALOG CMOS CIRCUITS

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## *Abstract*

*The paper shows the use of some methods of variability analysis to calculate how an analog CMOS circuit accuracy varies as parameters vary. Variability analysis is a technique by which one can determine, with good approximation, whether an analog circuit will work within the specification limits when some parameters vary between their limits. An application to a CMOS Operational Amplifier shows that it is able to consider simultaneously the effects of uncertainty of all of the parameters on a circuit accuracy, to provide strict bound (the min and max values) with only one evaluation and to perform sensitivity analysis.*

## I. INTRODUCTION

The parameters of analog CMOS circuits have tolerance limits, i.e. extreme values within which parameters values should lie. Tolerance limits include initial tolerance and drift due to age and environment [1]. If a resistor neither shorts nor opens but change in value either up or down by a large amount, it may cause significant enough changes in circuit performance to constitute a failure [2].

Recently it is presented [3] an excellent overview of methodologies that have become accepted industry standards for considering the piece part initial tolerance values and the effects of variations due to environmental conditions.

The methods and technique used are virtually the same as those used in a reliability analysis. The main difference is that a variability or error analysis is done to determine whether the circuits well or only in a mediocre fashion. In the case of reliability analysis the question one expect to answer is how often or what percentage of the time will the analog CMOS circuit be successful or unsuccessful [2].

The study of analog CMOS circuits with parameters that within the prescribed limits (e.g. measurement with accuracy guaranteed by manufacturer of measuring device) can be approached by Worst case, Monte Carlo, Method of Moments, Sensitivity Analysis, probabilistic Transformation of Variables or by Interval Arithmetic.

## II. DEFECTS AND FAULT MODELS OF ANALOGUE DEVICES

A fault is an imperfection in a device causing the device to behave differently than prescribed. The physical cause of the fault is often referred to as a defect.

Faults can be created during the design stage, during fabrication and during operation. Fabrication faults are usually unique for each single device or wafer and originate from processing defects, mounting, interconnections and packaging.

Processing defects are fabrication faults, which may be further, categorized depending on the strength of effect on the correct function or on the nature of the fault? A categorization of transistors faults nature is shown at figure 1.

Soft or parametric faults provoke a change in the circuit specification, which has limited effect on functionality. These are usually hard to detect and if detectable, expensive equipment is needed.

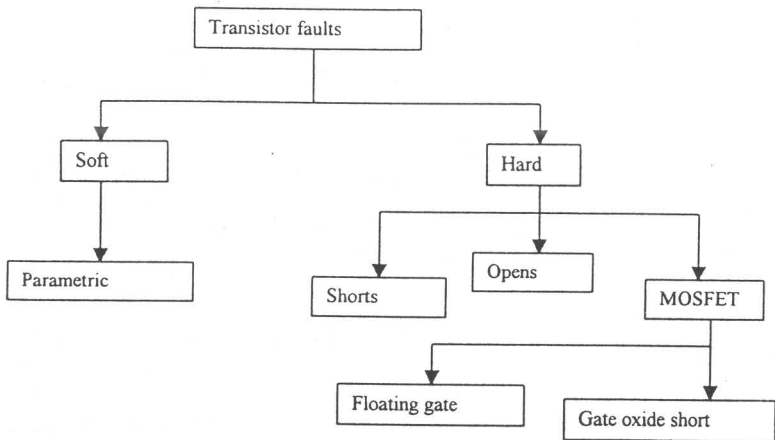


Figure 1. Nature of transistor faults

Hard or catastrophic faults may affect the functional characteristics of the system. They originate, for example, due to missing or spurious conductive paths in the integrated circuit structure. The majority of hard faults can be easily detected, but full detection is hard to achieve.

Using additional switches and resistors one can model transistor defects in PSPICE [1, 2]. This simple approach required manual or automatic rewriting of PSPICE input files and is considered inefficient. A better approach is to create a general fault model, which will switch to required fault on request from control input. All of the faults can be modeled by resistors of different values the fault model can base on voltage controlled resistors.

### III. TOLERANCE BANDS

Any slight random distortion always present, parameters of the manufacturing process vary over time and position of the wafer. Manufactures have to define an acceptable range of these parameters and hence the response of a good device to a particular input may vary within some tolerance band. It is essential to take into account this band when determine fault coverage, otherwise results will be over optimistic.

The simplest method of obtaining tolerance bands is based on a single run, which gives the curve, along with which the tolerances are set as constant or percentage values. The percentage envelope is not suitable for values crossing zero, as it would result in infinitely small tolerances.

A second method is based on the parameter sets for fastest, medium and slowest transistors, which are found from the measurements of a manufacturer. Simulations are carried out for these three sets and the maximum and minimum for each simulation step gives the tolerance envelope.

A third and potentially more accurate method is based on Monte Carlo simulation. This does not cover the parameter space fully, but is sufficient for a limited amount of parameters up to say four.

There is clearly an attraction to determining tolerance bands as accurately as possible. If the simulated band is narrowed than is the case in practice, test coverage figures will be over optimistic. Conversely, if the simulated band is too wide, coverage figures will be pessimistic. If a device is multi-sourced but the source for each device under test is identifiable, there are advantages to determining separate tolerance bands for each source as the worst case band including all possibilities, will be wider than any individual band. Most of the work reported to date has provided tolerance bands for the good circuit but based fault date on a single run. This is again a potential source of error.

#### IV. EVALUATION OF A LOW-VOLTAGE CMOS

If an analog CMOS circuit passes the Worst-Case technique it will never fail as long as the input parameters are maintained within the tolerance limits established by analysis [3]. Monte Carlo method requires more computer time than the others techniques. This uncertainty analysis provides a global view as it considers many possible combinations of the parameter\_value, rather than an exhaustive search of extreme values, which would require  $2^N$  solutions.

To test this concept and implement the approach in a real design is chosen. A design of low-voltage Operational Amplifier with improved characteristics like high open-loop voltage gain (above 100dB), large bandwidth (more than 4 MHz), rail-to-rail output swing, low input bias current, good common-mode rejection ratio and capability for offset voltage zeroing is investigated [3]. Crossed and parallel transistor are used in the input differential stage. Which results in reduction of the offset. The designed circuit is to be included in the cell library in order to be used in mixed digital-analog designs. The structure needs accurate behavioral analysis as well as to be laid out manually for  $2\mu\text{m}$  CMOS N-well ALICATEL MIETEC technology.

Fig.1 and fig. 4 show results for Monte Carlo and Worst Case respectively for uniform tolerance  $-50\%$ . Monte Carlo analysis for different channel weight but for the same tolerance is given at fig.2. At fig. 3, 5 and 6 one can see graphics of Monte Carlo and Worst Case respectively for tolerances of 1% and 5%, and 0,9V threshold voltage.

#### REFERENCES

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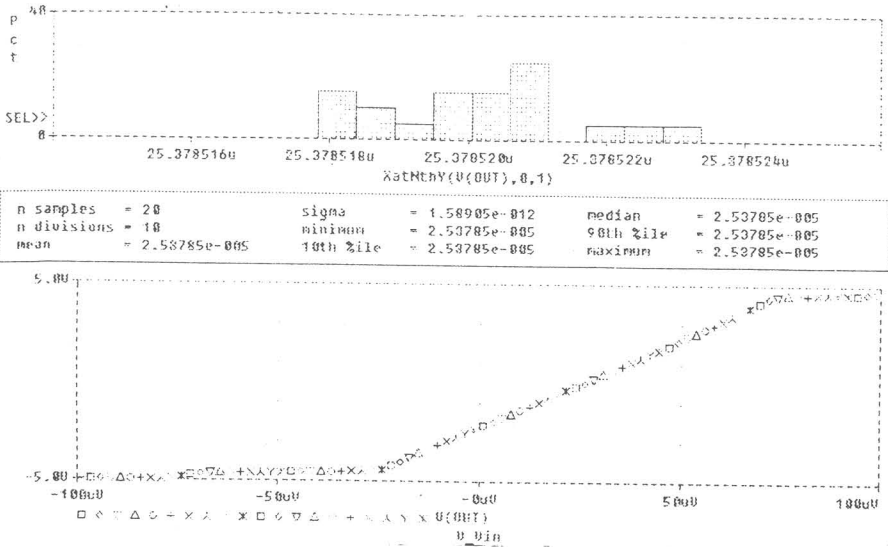


Figure 1. Monte Carlo analysis,  $L_{M1a}=L_{M1b}=L_{M1c}=10\mu\text{m}$ , tolerance - 50%

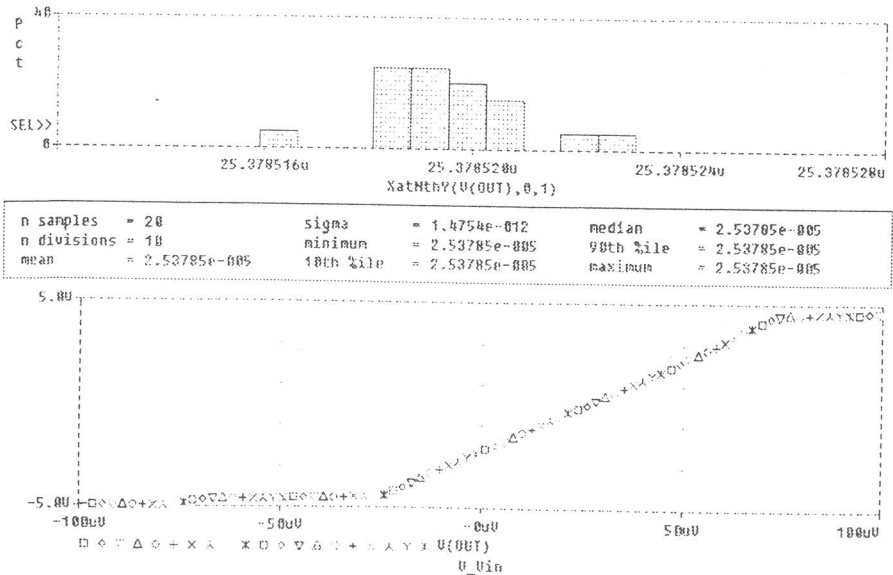


Figure 2. Monte Carlo analysis,  $W_{M1a}=W_{M1b}=W_{M1c}=40\mu\text{m}$ , tolerance - 50%

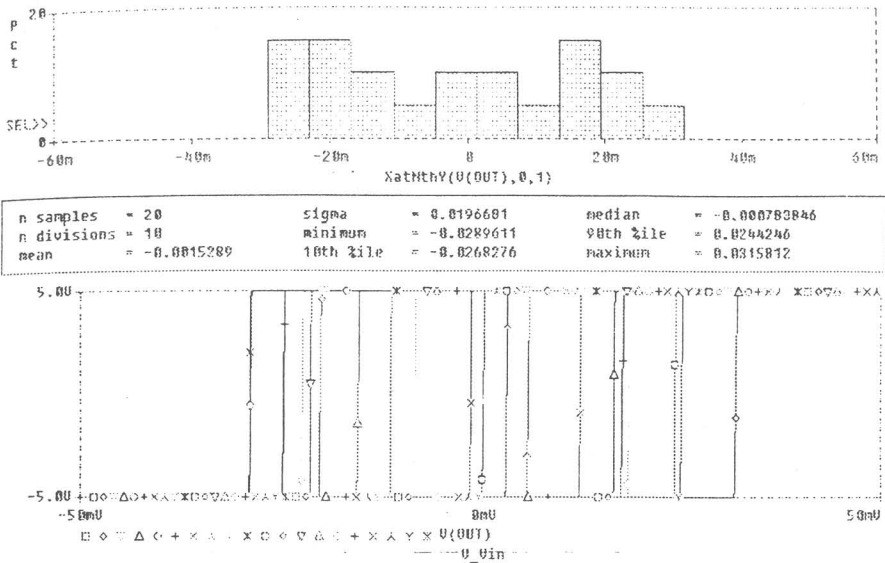


Figure 3. Monte Carlo analysis,  $U_{TOM1a}=U_{TOM1b}=U_{TOM1c}=0.9V$ , tolerance - 5%

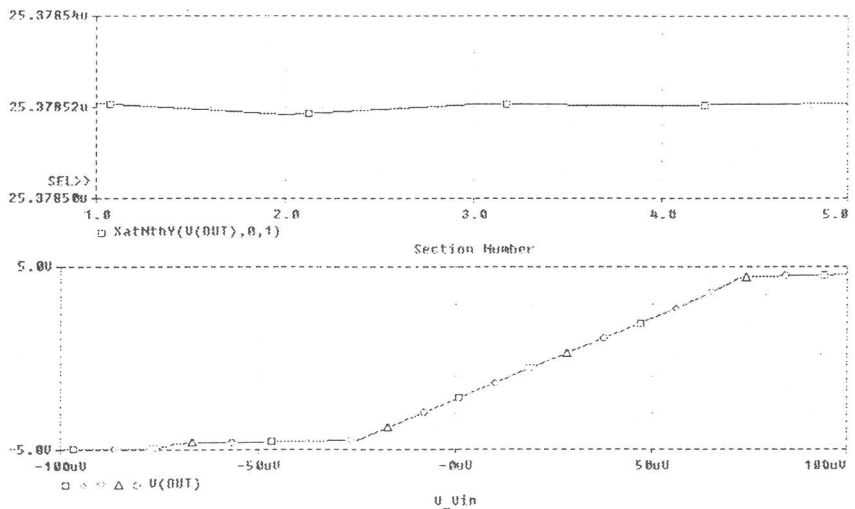


Figure 4. Worst Case analysis,  $L_{M1a}=L_{M1b}=L_{M1c}=10\mu m$ , tolerance - 50%

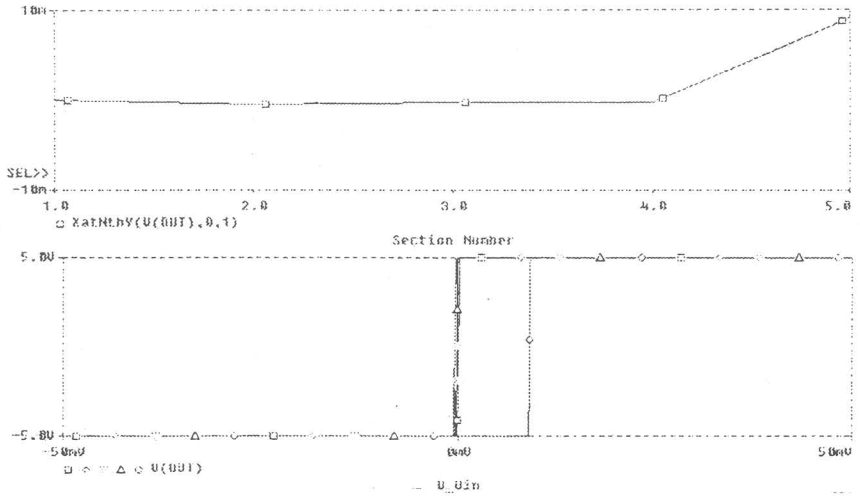


Figure 5. Worst Case analysis,  $U_{TOM1a}=U_{TOM1b}=U_{TOM1c}=0.9V$ , tolerance - 1%

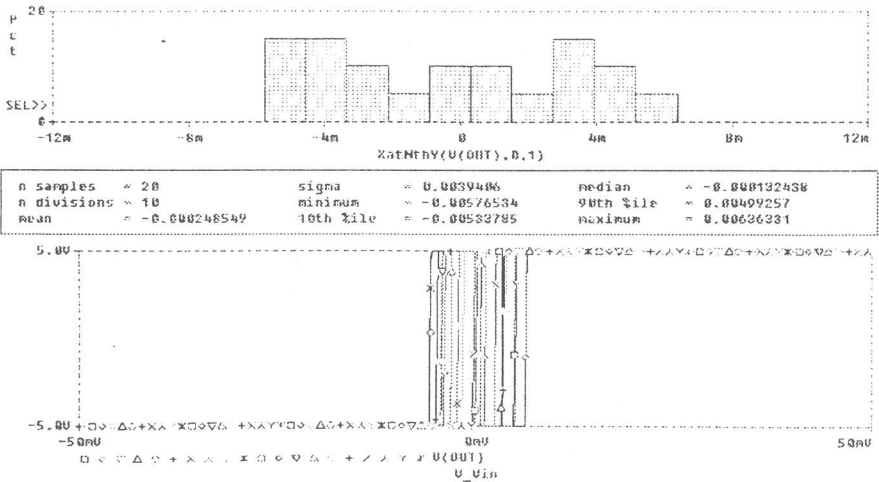


Figure 6. Monte Carlo analysis,  $U_{TOM1a}=U_{TOM1b}=U_{TOM1c}=0.9V$ , tolerance - 1%