Programmable Digital Device for Integrated Hall Sensor Signal Conditioning

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Abstract: ***Programmable Digital Device for Integrated Hall Sensor Signal Conditioning.*** *The paper addresses mixed-signal ASIC design implementation in intelligent sensor development. It presents a practical realization of the idea of integrating digital processor in an analog sensor. The ASIC design approach in solving the main problems is described in general, while the decision-making process is stressed. The programmable device presented has been developed to incorporate digital preprocessing of the signal in a Hall sensor using dynamic quadrature offset cancellation. Since it is intended to be integrated on one die with the analog sensor, the device ensures higher flexibility, easier adaptivity and extreme robustness of the intelligent sensor against mechanical stress. Throughout the project described below, top-down design approach has been employed, illustrating the application of hardware description languages in CAD process [3]. The device has been designed by the means of the hardware description language VHDL [4]. Logical simulation and synthesis software has been used extensively. The electrical circuit is synthesized by Synopsys Design Compiler using standard digital cells from the 2μm CMOS N-well Alcatel MIETEC technology library.*

Introduction: Nowadays there are more and more areas of signal processing where digital systems are used instead of analog ones. This is due to the many advantages of digital systems, among which are their flexibility, reliability and low cost. Furthermore, since the constant advance in microelectronics manufacturing technology allows realization of still more and more complex digital processing systems in an area same as before, the trends in the electronics branch are in wider spread of digital systems in signal processing.

In this connection, if the idea of incorporating digital signal processing to a sensor may have sounded inconceivable or at least extravagant a few years ago, now it is totally feasible easily and cost-effectively. Such a realization would result in a greater stability, which means that analog offsets, temperature shifts and mechanical stress will not degrade the sensor accuracy. Of course this is a great advantage especially for devices measuring static physical quantities. Moreover, if there is memory integrated where calibration data could be kept, output signal could be adjusted at any time, according to the needs of the system, a part of which it already is. In other words, the sensor could be used in various systems while the calibration could be done even after the final assembly. All those new features make the sensor better in terms of universalness, convenience and robustness.

The system treated in the following exposition is developed as a DSP to the analog Hall sensor from the article "Integrated Hall-sensor with Dynamic Offset Compensation" by K. Fillyov, T. Takov, Tz. Tzeneva and Sl. Neytchev. The goal is to show some basic concerns of the practical realization of a universal digital conditioning add-on to any analog sensor, and in parallel describe the features of the particular designed device.

Exposition: The general idea of the digital conditioning is to enable preliminary configuring of sensor output characteristics while keeping undegraded its dynamic range, linearity, sensitivity, and accuracy. Considering this, we must provide the system for performing all operations within the time gap between two subsequent conversions and must use operands with the necessary word lengths. Keeping configuration settings is the next main concern and it makes the use of internal non-volatile memory inevitable. Taking into an account that the memory should be externally erased and programmed, apparently we reach the conclusion that a tool to operate with it is necessary. Since the area of the analog sensor die is usually limited, and the number of pins reduced, the only reasonable decision is to construct an internal serial interface.

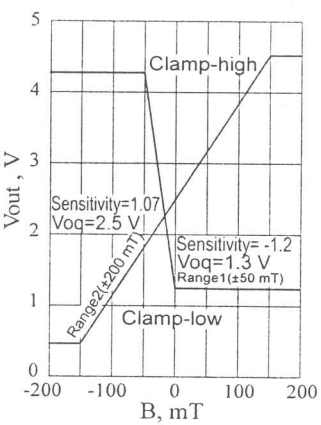

Fig1. Output characteristics of the intelligent Hall sensor

So the digital system we finally come to generally consists of three relatively functionally independent blocks as shown on the diagram below: the DSP, the memory and the serial interface. Of course AD and DA converters are necessary to provide the typical of mixed-circuit design analog to digital and digital to analog conversions. The converters we use are standard cells taken from Mietec 2 μm CMOS technology library: eight bit successive approximation ADC, and 8 bit DAC with resistor string. As an inevitable part of any digital system an internal clock generator is needed. Also an analog sensor measuring absolute temperature is necessary for the temperature compensation. A system detecting supply voltage under the minimum necessary for proper work of the DSP would guarantee the faultless work of the latter. Such a detector is optional and could be omitted without affecting the DSP functionality. Its assignment would be to activate reset signal when supply voltage drops under the permitted minimum.

1. The DSP has two parts working in parallel: the main signal conditioning channel and the block for linearization. In the intelligent sensor considered, the temperature drift of the Hall plate sensitivity and magnetic induction is left to be compensated in the digital device. The Hall voltage function of temperature could be presented in the following form: $V_H(T) \approx V_H(25°)(1+(TC_S+TC_B)\Delta T)$, where TC_S and

TC_B are temperature quotients of sensitivity and magnetic induction respectively. As a result of compensation the Hall voltage at normal ambient temperature ought to be obtained, and it is: $V_H(T_0) = \frac{V_H(T)}{1 + (TC_S + TC_B)\Delta T}$. By virtue of Taylor's polynomial approximation, we can replace rthe function above with the following expression: $V_H(T_0) = 1 - TC.\Delta T + TC^2\Delta T^2$, where $TC = TC_S + TC_B$. Since the same ADC is used for converting Hall and temperature voltages, assuming that temperature variation is much slower a process from the two, we can use the transducer channel with time separation. The continuity of the processing in the main channel is ensured employing a device that rejects temperature voltage replacing it with the average of preceding and succeeding values of hall voltage. The first and second order quotients of the polynomial are user-defined in the range of –128 to 127 and 0 to 127 respectively. The linearization block could also be adapted for compensation of any other slow or fast changing external phisical quantities, and so is universal. Sensor

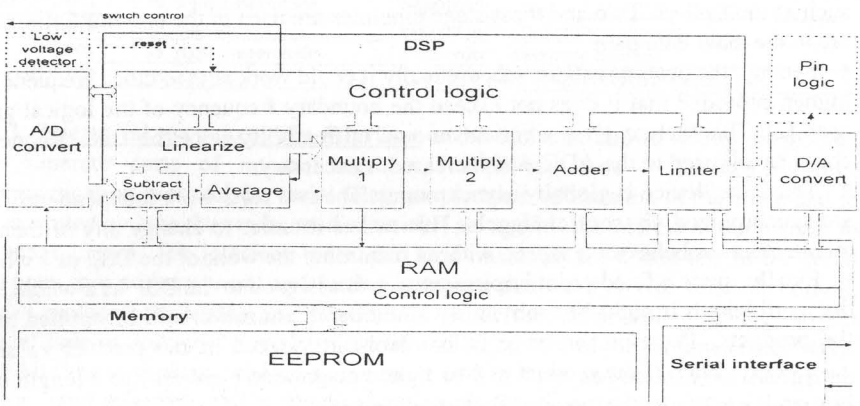

Fig2. Block diagram of the programmable digital device

sensitivity or the angle in the output characteristic is adjusted multiplying the linear Hall voltage with a user-defined quotient between ± 0,0625 and ± 3,97. The output quiescent voltage could be in the range of – 256 to 255. The lower and upper limit values are defined by the quotients of the clamping device and are from 0 to 255 for upper limit and from 0 to 127 for lower. After they are determined, the sensitivity may be calculated with the formula: $S = \frac{V_{upper} - V_{lower}}{Adc_{upper} - Adc_{lower}} \cdot \frac{256}{5}$, where Adc is the Hall voltage value after linearization. Once sensitivity is calculated, a value could be derived for the output quiescent voltage: $V_{OQ} = V_{upper} - \frac{Adc_{upper} \cdot S \cdot 5}{256}, V$. Register values are obtained by multiplying the respective voltages by 256/5.

There are some basic concepts applied to the DSP architecture design in order to provide the system for meeting the design goals.

- First, all the processes are serial: there are no universal devices for all multiplication or addition but on the contrary – all operations are performed by different specific devices working perpetually [1]. Thus a very high throughput of the DSP is achieved. Practically it produces new output on every ten clock cycles, which means that every ADC output results in a new DAC output. The high throughput of the DSP along with an increased clock frequency would allow measuring of considerably faster changing dynamic magnetic fields. Of course there is a price to be paid and this is the increased delay and area of the device. Moreover, with an increase of the ADC output (a typical example is twelve-bit Σ-Δ ADC) the amount of logical blocks for every operation inevitably increases with exactly the same ratio. While the delay, due to the increased logical depth, could be minimized introducing parallel structures, this would lead to further increase in the used area. Obviously a compromise between delay and area is necessary. The problem is solved optimizing all the parts for low area and introducing parallel structures in the critical sections, such as multipliers. Two and three stage pipelines are used in the two multipliers that are in the main data path.
- Second, the design is static – theoretically it could work at zero clock frequency or higher, provided that it does not exceed the boundary frequency of the logical gates used [2]. This feature gives a certain amount of flexibility since the clock frequency could be adjusted to the ADC, and increased if necessary.
- Third, the device is globally asynchronous. The two parts work independently and are synchronized via control signals. This makes it easier to change any of them in architectural or behavioral aspect, without disturbing the work of the DSP as a whole.
- Finally, since a fixed-point implementation is assigned to the DSP as a whole, and the word length is eight bits, obviously a number quantization will be applied to all the products. Therefore an error is inevitably introduced in the product value x: $\varepsilon = x - Q[x]$; Then if the product of two signed magnitude numbers has a length of L bits and $q = 2^{-L}$ is the quantization step, truncation would introduce an error of $-q < \varepsilon_T < q$, while rounding results in $\frac{-q}{2} < \varepsilon_R < \frac{q}{2}$ [1]. That is why rounding is incorporated to the two multipliers.

2. The memory block could be divided into two main parts – RAM and EEPROM. The random access memory is used to temporarily store configuration data before the latter is transferred in the non-volatile memory. In this way it allows user to test the work of the device and iteratively change some or all quotients' values untill the output characteristic matches the desired one. Then the programming could be done and configuration data – stored in the EEPROM. The memory block features a lock function. This is realized presuming that the initial value of the non-programmed or erased EEPROM cell is logical '1'. Then once a certain EEPROM cell, called by convention lock bit, is programmed, further erasing of the non-volatile

memory or reprogramming of the sensor is disabled. Locking of the sensor switches it permanently to analog output mode, blocking the serial interface and thus preventing memory from occasional reprogramming while elliminating the noise produced by the working interface. All the procedures of reprogramming the RAM or transferring its contents into the EEPROM are controlled by a logical block – a part of the memory block, interpreting the signals from the interface. By convention the memory is divided into different individually manipulated parts called registers. Every register stores data for only one of the user defined quotients.

Specification of intelligent sensor configuration registers

Register name and address		Register size and data coding	Register content
T0	111 ro	8b, two's complementary	Temperature sensor output at 25°C ambient temperature
Adc	111 ro	9b, signed magnitude	Linearized Hall sensor digital output
Dac	111 ro	8b, binary	Hall sensor digital output after conditioning
Lo	110	7b, binary	Lower limit value for the clamp
Hi	101	8b, binary	Upper limit value for the clamp
Voq	100	9b, two's complementary	Output quiescent voltage
Sens	011	7b, signed magnitude	Sensitivity
Sqtq	010	7b, binary	Second order temperature quotient
Tq	001	8b, signed magnitude	First order temperature quotient
Special	000	9b, binary	Lock bits, ADC innput range, addressing bits

3. The serial asynchronuos interface is the tool that allows writing or reading the separate parts of internal memory, called registers. It features its own communication protocol. Its serial telegram contains information of the command to be executed and the data to be read or written along with the address of the register to be manipulated. The interface is the part that translates the coded bits in the serial telegram into a binary word and further interprets that word or vice versa. According to the protocol, the logical zeroes and ones are defined as no voltage change within the bit time or voltage change between 60 and 90 percent of the bit time respectively. The bit time is constant, chosen in the range of 3 to 4 ms and defined via the first bit in the input telegram, called synchronization bit. The inactive state of the input and output is low and the telegram begins with the rising edge of synchronization bit. The end of the latter and the beginning of the next is marked by the first falling edge. From this point onward the bits in the serial telegram are separated by voltage change on the input pin. Employing this type of telegram allows input coding to be carried out through modulation on the supply voltage. An internal comparator is used to convert supply voltage changes into pulses with appropriate amplitude.

Three kinds of telegrams are defined in respect to the three kinds of commands that could be executed, namely write, read and special. All the three telegrams have something in common: they start with synchronization bit (logical 0), 3 bits for the command followed by a command parity bit and 3 bits for the register address followed by an address parity bit. In addition, every telegram has its differences:

- Write register telegram contains data bits and data parity bit after the address parity bit. The number of valid data bits is constrained to the size of the register with

the preceding address. It always ends with data parity bit after which the input level must go low. If the telegram is valid and the command has been processed, the interface answers with an acknowledge bit on the output. In case an arbitrary number of bits, not corresponding to the size of the register preceding address is let in, and occasionally no mistake is found during parity check, an acknowledge bit may not be released after the next telegram.

- Read register telegram ends with the address parity bit after which the input level must go low. If the telegram is valid and the command has been processed, the interface answers with an acknowledge bit on the output, followed by the respective number of data bits and a data parity bit. In this case the acknowledge bit defines output bit time.
- Special telegram also ends with the address parity bit after which the input level must go low. The difference is that the address could be of a randomly selected, though existing register. If the telegram is valid and the command has been processed, the interface sends specific control signal to the memory and in addition answers with an acknowledge bit on the output.

Serial interface command reference

Command name	Command code	Command description
Lock1	111	Permanently disables programming of T0 and part of Special registers
Lock	110	Permanently disables all commands by blocking the serial interface
Test	101	Measures the ambient temperature and writes it in T0 register
Erase	100	Erases the EEPROM before the next programming
Program	011	Programs the EEPROM with the content of RAM
Write	010	Writes a value to a register in RAM
Read	001	Reads a value from a register in RAM
(reserved)	000	-----

Conclusions: Transferring the logical design into an electrical circuit for evaluation purposes (using standard digital cells from the 2μm CMOS N-well Alcatel MIETEC technology library) resulted in a redundancy of consumed area – it turned out to exceed ten square μm. With the powerful tools for ASIC design, namely Synopsys Design Compiler, it was further optimized and number of simple logical gates reduced by almost one third. Still bearing in mind that a submicron technology implementation certainly would reduce consumed area, we can conclude that the device is practically realizable, even if it introduces some new problems concerning mixed-signal design.

References:

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