

HIGH VOLTAGE POWER SUPPLY SYSTEM FOR ENDCAP MUON STATION ME1/1 OF THE LHC CMS DETECTOR

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The Cathode Strip Muon Chambers (CSCs) in each endcap of the CMS detector are organized in a few groups, called stations. The first group – ME1/1 – consist of 36 CSCs in each endcap. In order to increase the precision of the measurements each chamber contains 6 layers with independent read-out electronics and HV power supply

A more economical solution for the HV-system is accepted - one HV-channel will supply the corresponding layers of two neighbouring CSCs. Thus the total number of HV channels for both ME1/1 stations is decreased to 216. The basic unit of this system is a 12 HV-channel module. Six modules with one Crate controller are accommodated in one 6U Eurostandard crate. The whole system has three crates, controlled by an IBM-NT host computer via a serial RS-485 interface. This computer is also connected to the global detector slow control system SCADA. The block diagrams of the crate, HV-module and crate controller are described.

The two endcap muon stations ME1/1 are an important part of the CMS detector for the new CERN¹ accelerator LHC [1,2]. They are in each station 36 Cathode Strip Muon Chambers (CSCs), separated in two groups of 18 – forward and backward (F, B, fig. 1). Each CSC contains 6 counting layers [3], needing individual high voltage (HV) supplying (Fig. 2). In order to decrease the total number of HV channels the corresponding layers of two neighbouring CSCs (of the same group – B or F) are fed by one common HV power supply channel. Thus, the total number of HV channels for one endcap ME1/1 station is 108, i.e. 216 channels for all system.

The structure of the ME1/1 HV system is shown on Fig. 3. It is based on 12 HV-channel 6U Eurostandard modules. Six 12-channel modules are accommodated in one 19” Eurostandard crate. There are in each crate one Crate controller, providing computer control and settings of each HV channel. Three HV crates are needed for both ME1/1 stations. These crates together with a spare crate are disposed in two standard racks located in the control room at a distance of about 110 m from the detector.

Each module supplies 4 CSCs through two 22-contacts connectors, connected in parallel: one 22-wires cable feeds two neighbouring CSCs – one from group F and one from group B, using a HV-distributor mounted on the B CSC.

The HV system is controlled by a PC-NT computer through a serial RS485 interface, using a custom designed software. The channel number, its output voltage and current as well as the voltage and current limits are displayed on the monitor. The interface with Detector Control System SCADA is realized by a DIM-server.

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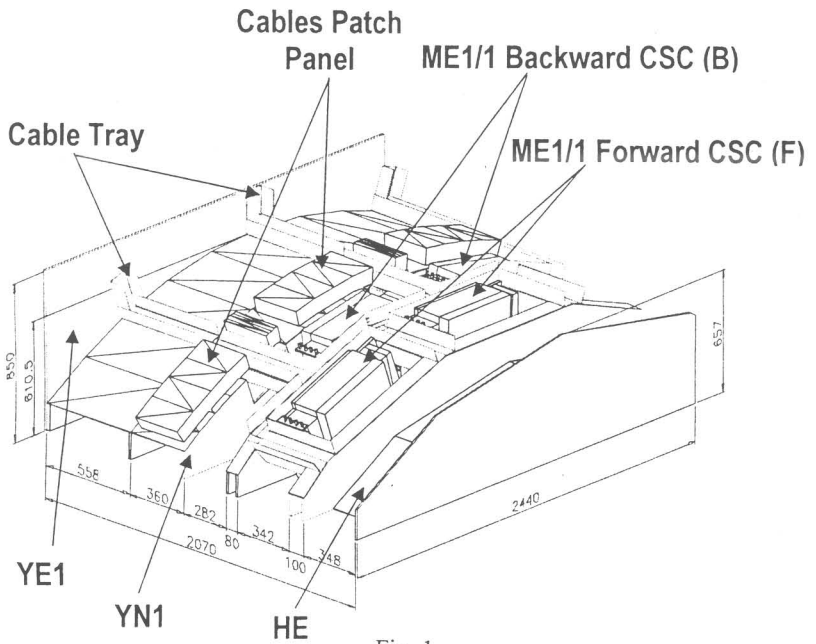


Fig. 1

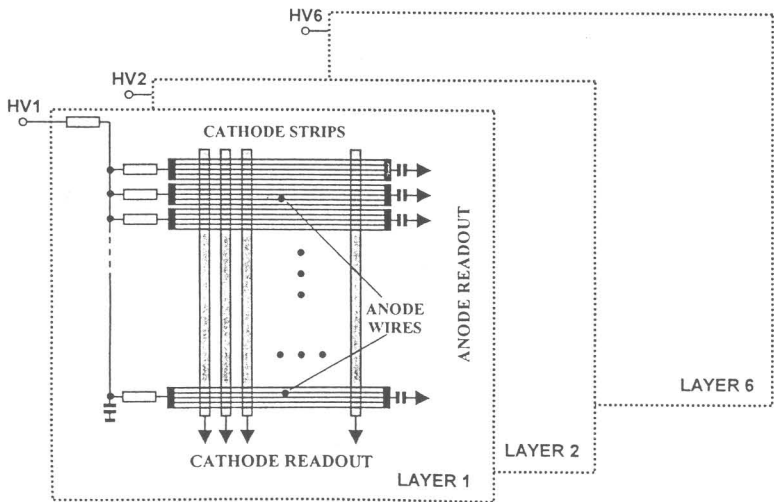


Fig. 2

The block diagram of the crate is shown on Fig. 4. The crate power supply provides 4 voltages: +40 V (V40p), +5 V (V5p), +12 V (V12p) and -12 V (V12n) as well as a high stability reference voltage of +5 V (Vref).

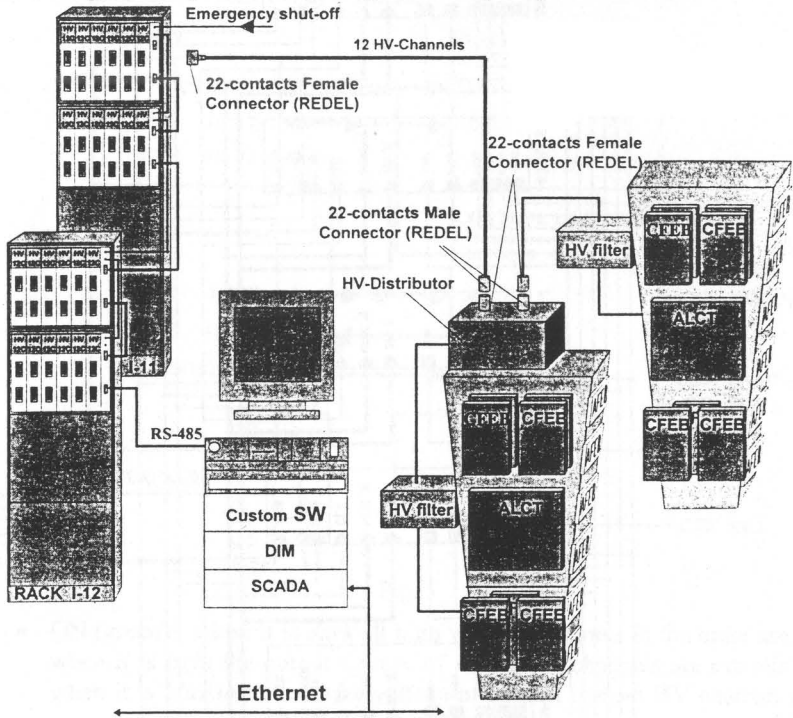


Fig. 3

The 6 modules in the crate operate under control of the Crate controller (see Fig. 5). It addresses the modules by a four line bus (MD) and determines the operation (write to addressed (or to all) module(s)), read from addressed module, send instructions to addressed (or to all) module(s)) by a three line bus (S). The data exchange is in serial mode (D_{OUT} , D_{IN} , CLK). The reset line is provided for emergency shut-off of the HV channels in all modules (at outside KILL command).

The block diagram of the Crate controller is shown on Fig. 5. Through the CONTROL LOGIC block it checks the status of the HV channels, controls the output voltages, reads the value of the output voltages and currents as well as the voltage and current limits and stores all these values in the MEMORY. Thus, when the host computer addresses the controller, it is ready to transfer the required information. The controller CPU is an Intel single-chip microcomputer (I 8031). As is mentioned above the serial interface RS485 is accepted as a link between the

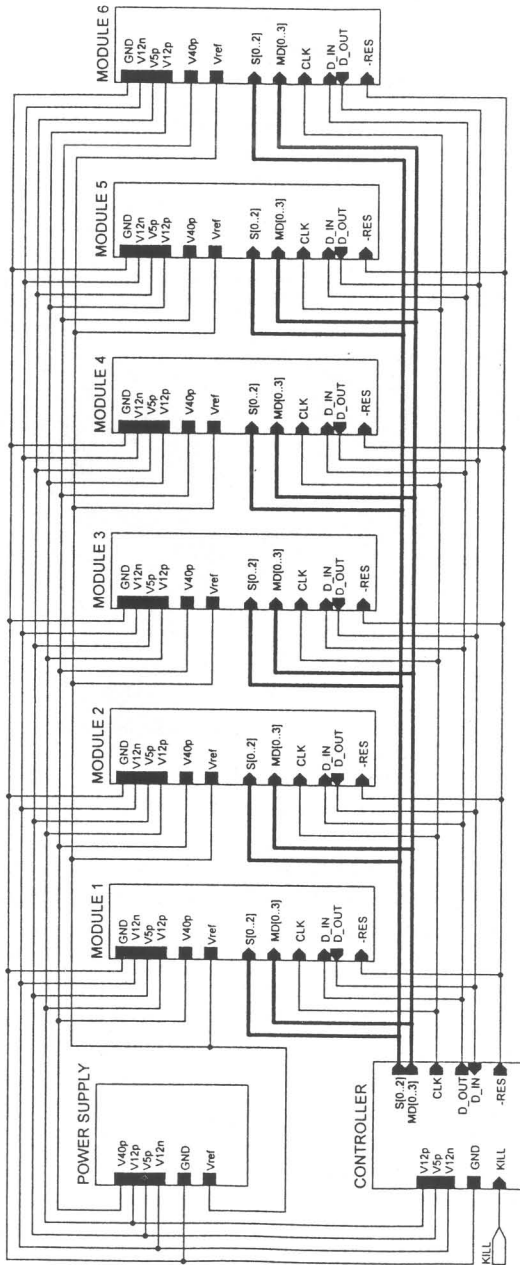


Fig. 4

Crate controller and the host computer. By means of the STATUS DISPLAY block the status of the system is shown by 5 LEDs:

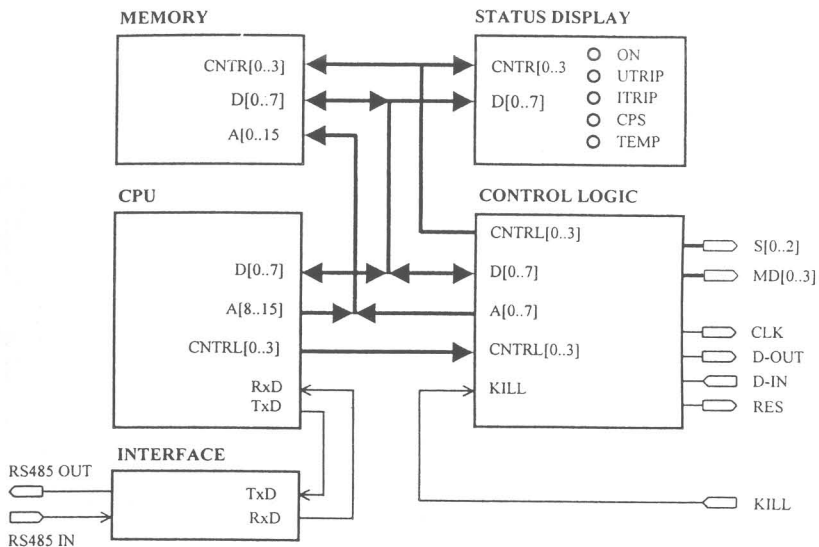


Fig. 5

- ON (green): when it is *dark* all high voltage channels in the crate are off; when it is *light* the output voltage of all set HV channels are established; when it is *blinking* the output voltage of at least one set HV channel is in course of establishing (increasing or decreasing);
- U_{TRIP} (red) – at least one voltage protection is activated;
- I_{TRIP} (red) – at least one current protection is activated;
- CPS (red) - at least one of the crate power supply voltage values is out of range;
- TEMP (red) – the inside temperature of the crate is above 50°C .

The block diagram of the 12 HV-channels module is shown on Fig. 6. In each channel an individual circuit for regulation and stabilisation of the output high voltage (HV1, channel 1) is used. In the output block (RFD), the HV1 is provided by a four-stage voltage multiplier, rectifying and multiplying the output voltage of a generator-transverter (GT). The supply voltage of GT is provided by a pulse-wide modulation voltage regulator (PWM) with an inner protection circuit.

At normal operation the PWM is controlled directly by the DAC output voltage (corresponding to the set HV1 value) and by HV1 (i.e. by UO1, received from HV1 by means of the feedback divider) through the operational amplifier OA1 and the diode D1. In case of a current overload ($IO1 > I_{LIM1}$) the output voltage is decreased by the OA2 (comparing IO1 and I_{LIM1}) in order to keep up $IO1 = I_{LIM1}$. In

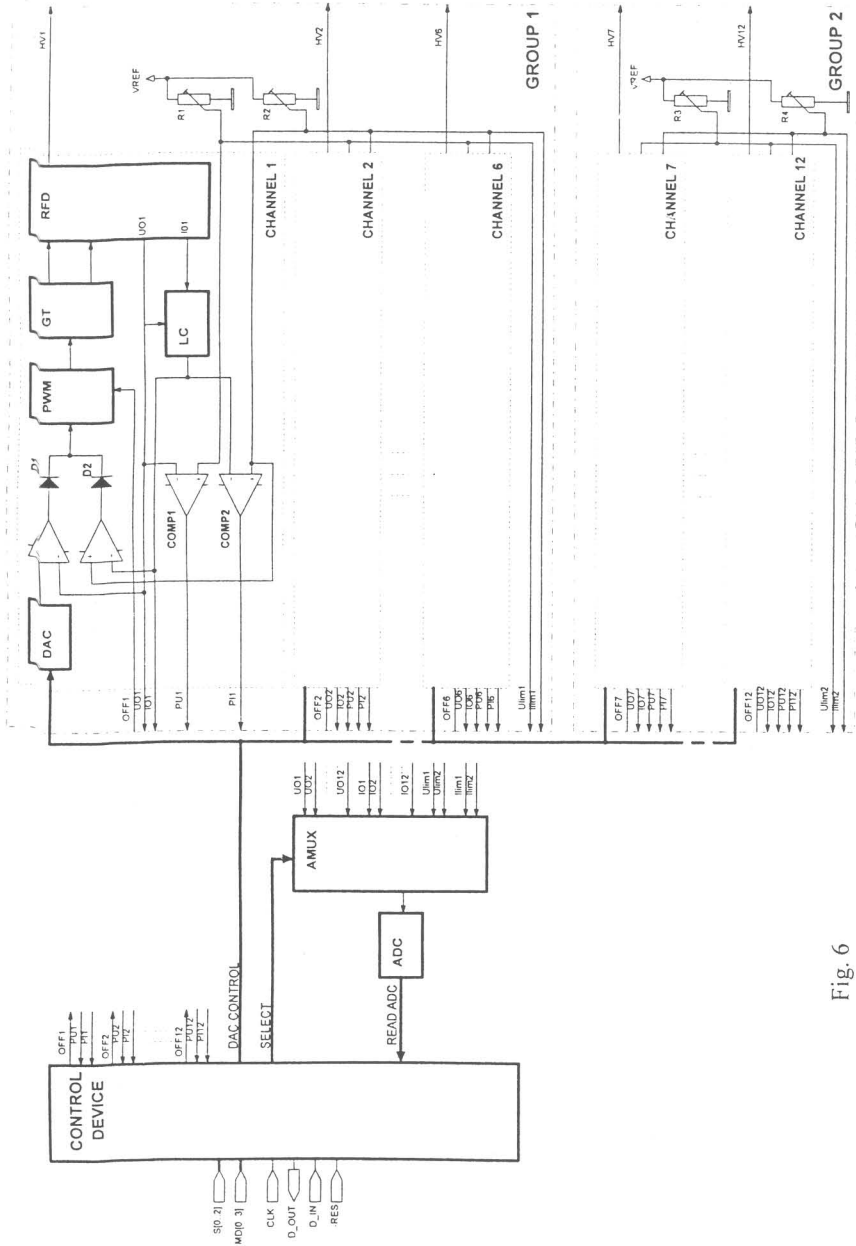


Fig. 6

the same time an alarm signal (PI1) is produced at the output of the comparator COMP2. When an over voltage is come out $UO1 > U_{LIM1}$, the output signal (PU1) of the COMP1 switches off the channel (by means of the CONTROL LOGIC) and the output voltage goes to 0 with a rate, determined by the output time constant.

Two analog signals from each channel (UO_i , IO_i) as well as the voltage and current limits of the two groups of 6 channels (U_{LIM1} , I_{LIM1} , U_{LIM2} , I_{LIM2} , set by R1, R3 and R2, R4) are fed to the analog multiplexer AMUX in order to be switched to the analog-to-digital converter ADC. From ADC output their values are transferred to the Crate controller for storage. In order to provide the necessary precision of setting and measuring all of these values 12 bit DAC's and ADC are used.

The operation of the module is managed by the Crate controller through the CONTROL LOGIC.

The technical parameters of the HV power supply are as follows:

Channel technical parameters:

- Output voltage range 0 ÷ 4000 V;
- Output polarity positive;
- Output current range 0 ÷ 0,4 mA;
- Temperature stability < 100 ppm/^oC
- Long term stability < 0,1%;
- Voltage ripple < 50 mVpp.

Module technical parameters:

- Number of channels 12;
- Setting of upper output voltage and current limits for each group of 6 channels manually;
- Monitoring of the set voltage and current limits yes;
- Output voltage ramp up/down for all channels in the module 100 - 2000 V/s.

Crate technical parameters:

- Number of modules 6;
- Number of channels 72;
- Crate controller 1;
- Total mains power consumption 220 VA.

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