Fast ISA-Bus multi-channel analyzer

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Abstract

Fast nuclear spectroscopy multi-channel analyzer is described. It works with NaI(Tl) scintillation detectors at high-count rates and is performed as an ISA-Bus card. The module consists of an input buffer, constant-fraction discriminator, fast dual-slope ADC (gating integrator), control block, dual-port memory and high voltage power supply unit for photo-multipliers. Figure 1 is the block diagram of the analyzer and figure 2 shows the schematics of the input buffer, the constant-fraction discriminator and ADC.

The constant-fraction discriminator marks the occurrence of the input pulse independent of its rise time and amplitude. It uses a Bessel filter as a 30 ns delay line and two comparators. The first one is the level comparator. The second one is a zero-crossing comparator. It compares the delayed signal with the 30% fraction of it. The output pulse of this comparator is used to start the integration.

The fast dual-slope ADC integrates the input pulse in 1 us and has a maximum disintegration time of 4 us. It is a dual-scale ADC. If the input pulse is under ¼ of the range, the disintegration current is 250 uA instead of the nominal current of 1 mA. So the analyzer accumulates simultaneously two specters: one 256 channel (first ¼ of the range) and one 384 channel (the rest of the range).

The output signal of the input buffer is filtered using simple RC filter with 220 ns time constant. This time constant is near the decay time constant of the NaI(Tl) scintillator. The filtered signal is converted to current and this current charges the integrating capacitor C6 trough the current switch Q3Q4 and the current mirror Q1Q2. The current switch is opened 1 us after the start of the conversion. At the end of this time the control block checks the state of the comparator U2A and starts the

disintegration. It opens the switches Q7Q8 or Q9Q10. The comparator U2B works as a zero-crossing detector. When the voltage of C6 crosses the zero the conversion is done. The MOS transistor Q6 resets C6 after the conversion.

The control block performs all control functions. It is implemented into one Spartan 05 FPGA. The control block checks the outputs of the comparators, drives the current switches, accumulates the spectra in the dual-port memory and generates an interrupt request every 6 seconds. The clock frequency is 64 MHz.

The dual-port memory is split on two banks. Every 6 seconds the controller accumulates spectra into one of them. It uses both outputs of one flip-flop to switch between banks. The non-inverted output is used as LA9 and the inverted one is used as RA9. The other bank is visible from the ISA-Bus simultaneously.

The high voltage power unit delivers up to –2048 V and is software controlled using 12 bit DAC. This way it is possible to stabilize the spectra. The maximum output current is 2.5 mA.

The multi-channel analyzer has been used as ash-content meter of the coals on transport belts in thermal power plants and tested up to 160000 events per second output count rate.

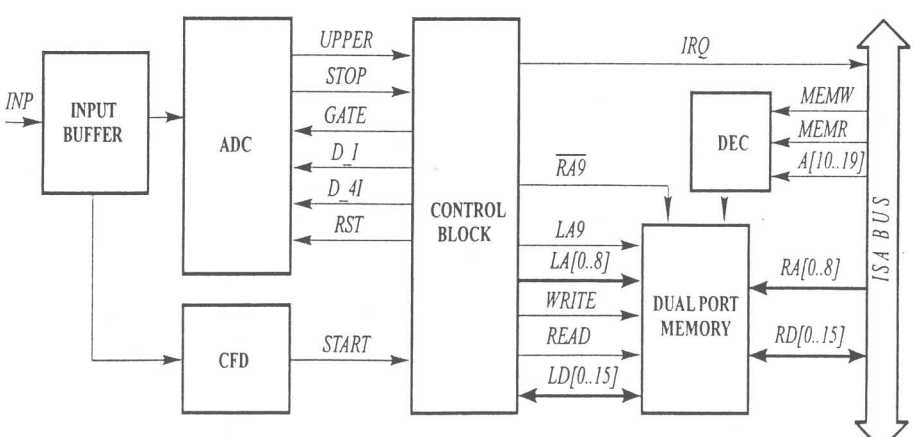

Figure 1

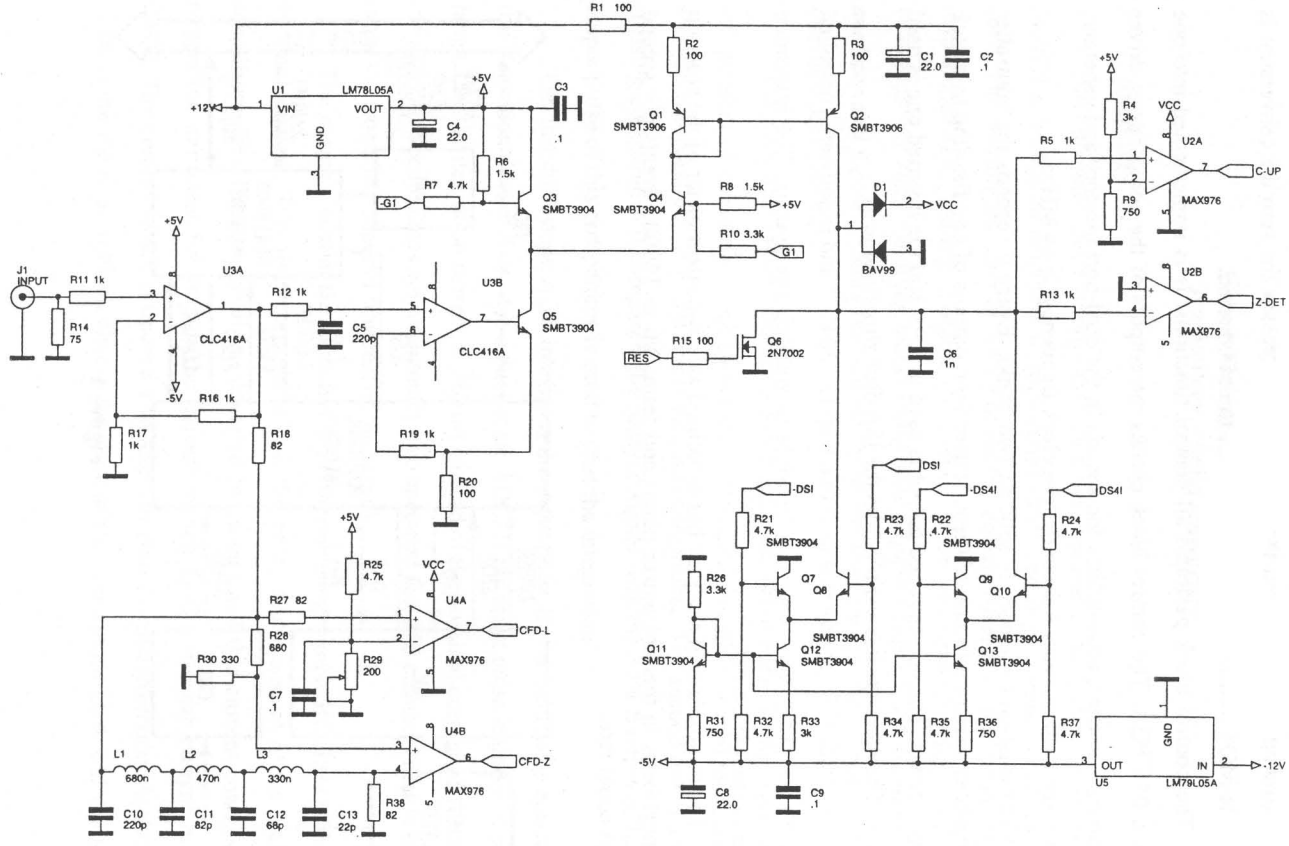
R1 100
R2 100
R3 100
C1 22.0
C2 .1
U1 LM78L05A
VIN
VOUT
GND
+12V
C3 .1
C4 22.0
+5V
R6 1.5k
R7 4.7k
-G1
Q1 SMBT3906
Q2 SMBT3906
Q3 SMBT3904
Q4 SMBT3904
R8 1.5k
R10 3.3k
G1
D1
BAV99
VCC
R4 3k
R5 1k
U2A
MAX976
C-UP
R9 750
U2B
Z-DET
R13 1k
J1 INPUT
R11 1k
R14 75
U3A
CLC416A
R12 1k
C5 220p
U3B
Q5 SMBT3904
R15 100
RES
Q6 2N7002
C6 1n
-5V
R16 1k
R17 1k
R18 82
R19 1k
R20 100
DSI
-DSI
DS4I
-DS4I
R21 4.7k
R22 4.7k
R23 4.7k
R24 4.7k
R25 4.7k
R26 3.3k
R27 82
R28 680
R29 200
R30 330
C7 .1
U4A
U4B
CFD-L
CFD-Z
Q7
Q8
Q9
Q10
Q11 SMBT3904
Q12 SMBT3904
Q13 SMBT3904
R31 750
R32 4.7k
R33 3k
R34 4.7k
R35 4.7k
R36 750
R37 4.7k
L1 680n
L2 470n
L3 330n
C10 220p
C11 82p
C12 68p
C13 22p
R38 82
C8 22.0
C9 .1
OUT
IN
-12V
U5 LM79L05A

Figure 2