

DAQ for CMS RPC chambers test

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Part of the Resistive Plate Chambers (RPC)[1] for the barrel muon system of the CMS detector at LHC accelerator at CERN will be produced by CMS Sofia collaboration and tested in cosmic muons in order to study their performance at different running conditions. The data acquisition system (DAQ) developed to handle the signals generated by the RPC is described.

Introduction

The Compact Muon Solenoid (CMS)[2] Collaboration has chosen the Resistive Plate Chambers as dedicated detectors for the first level muon trigger system. The RPC are gaseous parallel-plate chambers that combine a reasonable level of spatial resolution with excellent time resolution, comparable to that of scintillators. An RPC consists of two parallel plates, made out of phenolic resin (bakelite) with a high bulk resistivity, separated by a gas gap of 2 millimeters. The whole structure is made gas tight. The outer surfaces of the resistive material are coated with conductive graphite paint to form the HV and ground electrodes. The read-out is performed by means of aluminum strips separated from the graphite coating by an insulating PET film. The RPC

proposed for CMS is made of two gaps with common pick-up strips in the middle, the so called double gap RPC. In this case the total induced signal read out by the Front End electronics is the sum of the two single-gap signals. The chambers will be operated in the so called avalanche mode with 96% $C_2H_2F_4$ based mixture and 4% $i-C_4H_{10}$. The RPC produced by CMS Sofia collaboration are $250 \times 150 \text{ cm}^2$ in area and have 2×96 read-out channels per chamber.

The RPC has to fulfill three basic requirements: good time resolution, high efficiency and uniformity and low cluster multiplicity. To test the performance of the RPC, a dedicated experimental set-up will be developed. Five chambers will be placed between two trigger scintillator layers able to determine the impact point on the RPC of the incoming cosmic muons, so the total number of readout channels will be 960. The efficiency will be defined as the ratio between counting rate of the signals and trigger rate.

In this report we describe the specific readout system designed to process the RPC signals.

The readout system

Each chamber is equipped with 12 Front-End boards. Each board handles signals from 16 strips. A single channel consists of two-stage amplifier, threshold discriminator, one-shot and line-driver. At the output a LVDS signal is generated over twisted pair copper. The signal has a voltage of 250 mV on 110 Ohms. They are read out when the trigger signal creates a 25 ns gate by 5 x 2M CAMAC modules. To handle the signals in the fastest possible way some of the logic functions required for the trigger are already performed on the readout board. The block diagram of the readout system is given on fig. 1.

The CAMAC modules (fig. 2) are designed to convert the LVDS signals into TTL signals and then to transfer them by the serial SPI bus. 16 bit translators SN75LVDT386[3] from TEXAS INSTRUMENTS will be used. For

conversion of 96 parallel input signals to SPI will be used the FastFLASH XC95144XV High-Performance, Low-Power chip from Xilinx[4].

The aim of the module SPI (fig. 3) is to receive from the Xilinx chips by SPI bus information for the flashed strips and to convert parallel information into number of strip and number of chamber and by serial RS232 port to transfer information to the personal computer for further analysis. Working frequency of SPI is 1MHz and 960 strips signals will be transferred and converted in about 1 ms. RS232 port will transfer from 9600 to 115200 Kbps information and it is sufficient for the test in cosmic muons (~ 70 muons/m²*sec). The incoming data will be processed by the PC using LabVIEW from NATIONAL INSTRUMENTS.

References

1. The Muon Project, Technical Design Report, CERN/LHCC 97-32, CMS TDR 3, 15 December 1997.
2. The Compact Muon Solenoid (CMS), Technical Proposal, CERN/LHCC 94-38, LHCC/P1, December 1994.
3. SN75LVDT386, HIGH-SPEED DIFFERENTIAL LINE RECEIVERS, Copyright 1999, Texas Instruments Incorporated.
4. FastFLASH™ XC9500XV High-Performance, Low-Power CPLD Family, January 19, 1999 (Version 1.0), XILINX.

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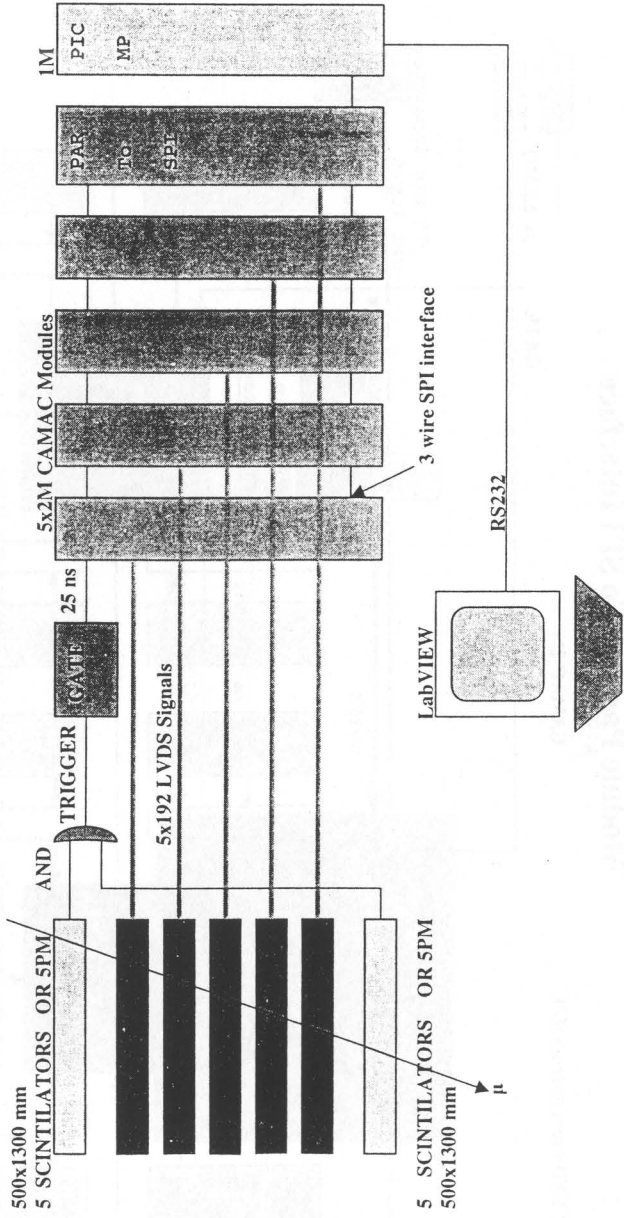


Fig.1

Module Parallel To SPI Interface

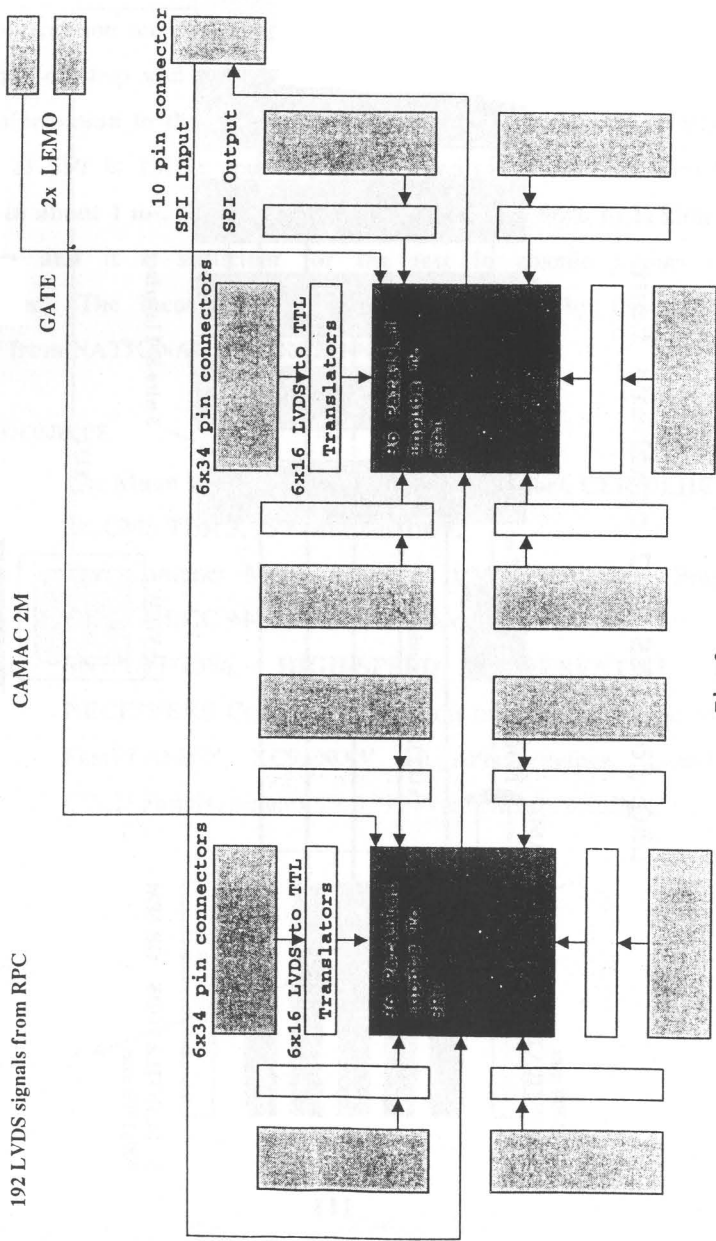


Fig. 2

Module SPI To RS232 Converter

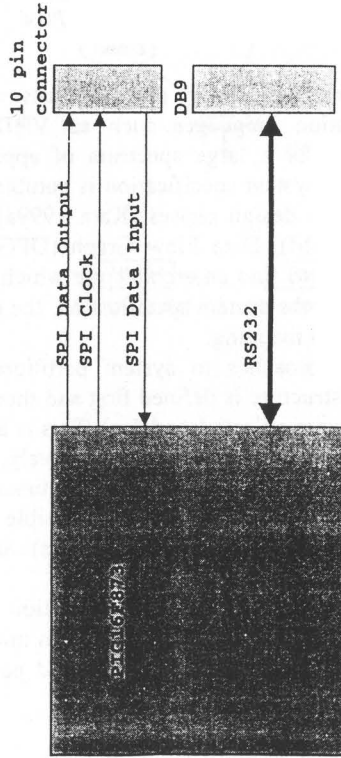


Fig. 3