TESTING THE NELINIARITIES OF THE DIGITAL TO ANALOG CONVERTERS USING LABVIEW ENVIRONMENT

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The paper presents some considerations about testing the quality parameters of digital to analog converters (DAC) and describes a practical realised system used for testing the neliniarities of DAC converters.

1. Introduction

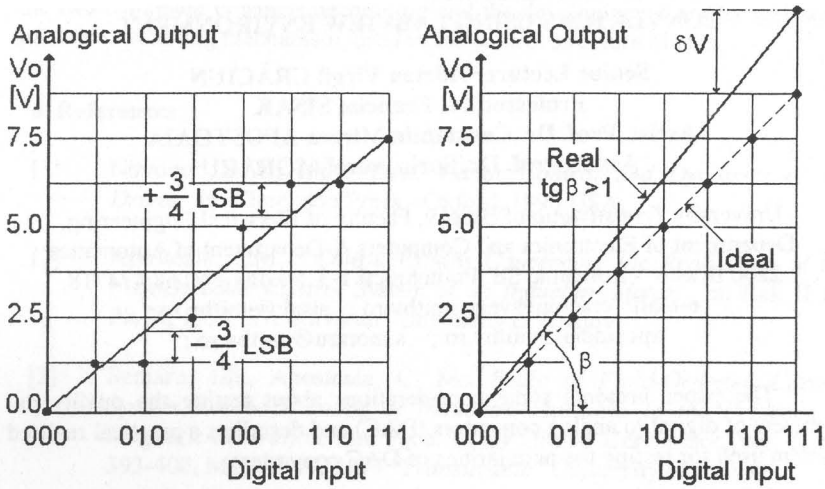
Testing mixed signal integrated circuits (IC) is a difficult task. While the digital test has earned enough maturity in terms of the availability of CAD tools and structured test strategies, the mixed signal test is still complex. Typically, mixed signal circuitry represents around 20% of a mixed-signal IC area while its corresponding test cost represents 70% of the overall test cost [1].

Data converters are typical mixed-signal circuits that bridge the gap between analog and digital signals. They determine the overall precision and speed performances of the system and therefore dedicated test techniques should not affect their specifications. For instance, it is difficult to test the analog and the digital portions of data converters separately using structural test methods and conclude that the whole device specifications are respected. Therefore, it is necessary to test data converters as an entity using at least some functional specifications. There is also a strict requirement in terms of precision related to hardware used to test data converters.

2. Data Converters Parameters

The quality parameters for data converters can be divided in relative and absolute parameter [2]. From the relative parameter category the integral linearity analyzed in figure *1a* (for a 3 bits, 10V DAC) is ±3/4LSB (Less Significant Bit). The error was considered based on the line between the extreme points, not with the best-fit line. This definition is more convenient in the computer-based systems, because the system can automatically adjust this error.

From the absolute parameters category, the full scale (or gain) error was presented in figure *1b* for a 3 bit, 10V DAC. In this case the error has a positive value δV.



a) Integral Neliniarity *b) Gain Error*

Figure 1. *DAC Parameters*

3. System Hardware

The system block diagram is presented in figure *2*. The system is based on a personal computer equipped with an acquisition board, an interface between that board and the tested DAC. The interface consists on a voltage to current converter and a current to voltage converter because the acquisition board operates with voltages and the DAC under test is a current one. An analog multiplexer placed between the DAC and the I/V converter selects one of the two outputs of the DAC to be tested.

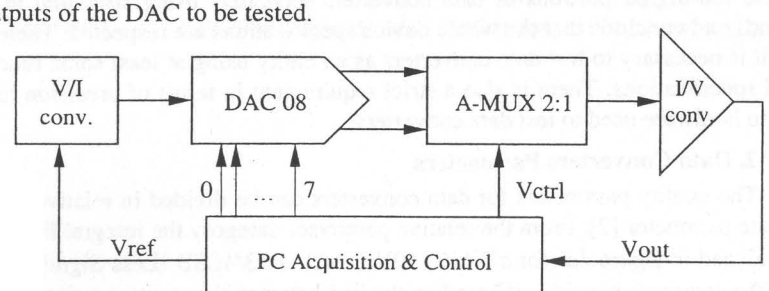


Figure *2*. *The Block Diagram*

From the testing point of view the circuit perform a functional testing using the analysis of the structure of the circuit and/or a complete functional testing from the neliniarities point of view. The testing system is an external one, connected at integrated circuit pins.

The interface principle schematic is presented in figure *3*. Practically, the

A-MUX was realized with 2 analog DMUX 1:2 (2/3 of MMC4053 CMOS circuit) for the 2 outputs of the circuit, because when one of the outputs is selected, the other one must be grounded. The DMUX is controlled with the V_{CTRL} voltage applied using a logic level adapter (from TTL to CMOS, not figured). The analog switch 'on' resistance is $R_{on} \leq 150\,\Omega$ for this CMOS circuit [3]. The lower supply voltage of the DMUX is a negative one:

$$V_{EE} \leq -\left|I_{ODAC\,\max} \cdot R_{on}\right| = -\left|4m \cdot 150\right| = -0.6\,V \qquad (1)$$

The V/I converter was realized with the precision resistor R1 using the DAC input operational amplifier and the I/V converter was realized using a precision OpAmp (AO) with an offset compensation circuit with P1. The slew rate (SR) of this AO is the main limitation for the maximum speed of the system.

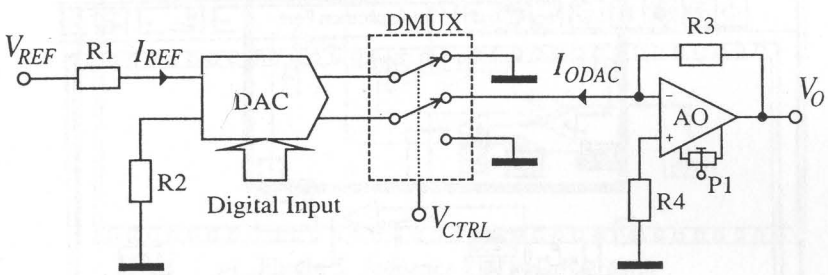


Figure *3. The Acquisition Board - DAC Interface*

For the circuit to preserve the DAC transfer factor, the I/V and V/I converters must have the same conversion factor. To realize this the resistors used in the circuit must be very well matched:

$$R1 = R3 \quad \pm 0.1 \ldots 0.5\% \qquad (2)$$

The precision of the system depends also on the reference voltage precision (better than 0.1% for the 12 bits DAC from the acquisition board [6]). The offset error of the AO must be less than a tenth of the minimum LSB value. For the minimum reference current $I_{REF\,\min} = 0.25\text{mA}$ and for the 8 bits DAC, the LSB is $I_{ODAC} \cong 1\mu\text{A}$ and $V_{O\,\min} \cong 2\text{mV}$. The R2 and R4 resistors are used to reduce the offset errors for the DAC input OpAmp and for the AO.

Considering the precision and the facilities offered by the PC acquisition board [6] (type AT-MIO-16E-10), this hardware interface was easy to design and execute and can be easily adapted for a different DAC type.

4. System Software

The software for this system was realized using the LabView graphical programming language G. In this environment the algorithm branches are solved concurrently when possible. It was chosen a solution of a sequential algorithm presented in figures *4,5* and *6*. There were 4 sequences:

- Sequence 0 of the program is the initialization block. The 8 bits digital I/O (of the acquisition board) were used as an 8 bits data bus, the 2 analog out-

puts were used: one for reference voltage (V_{REF}) generation and the other one for controlling the A-DMUX (V_{CTRL}).

- Sequence 1 computes and display (on the front panel, figure 7) the voltage for the full scale (digital input '0' and V_{CTRL} ='1', or digital input 'FFFF' and V_{CTRL} ='0'), 'V255' and the voltage step, 'V01', corresponding to the full-scale value. That means, from the theoretical point of view, the use of the line between 0 and maximum value at the DAC output, when computing the integral neliniarity, as shown in figure *1*. In this sequence it is also computed and displayed the absolute error for the full scale as a voltage, 'dV255' and as a percent 'dV(%)'.

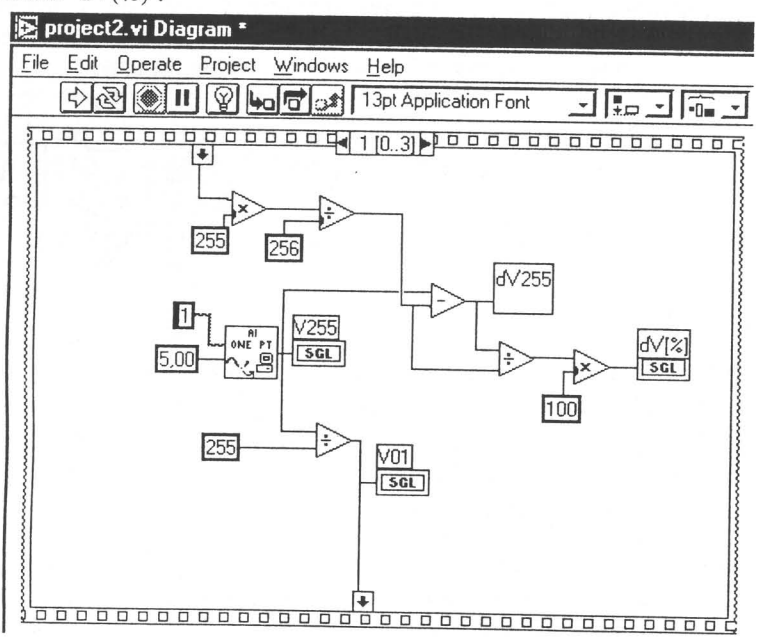


Figure *4. Sequence 1 of the program*

- Sequence 2 computes and displays on a graph the error (expressed in fractions of LSB) for each bit of the DAC separately. There was applied 9 different binary combination at the DAC input.
- In the last sequence of the program (sequence 3) there were acquired and displayed the voltages for all the possible binary combinations. It was also computed and displayed on a graph, the integral error for every bit combination. The maximum integral error of the DAC and the bits combination where this error comes were determinate, memorized and displayed in the maximum relative error area of the front panel.

Figure 7 presents the front panel of the virtual instrument (VI) realized using the presented algorithm.

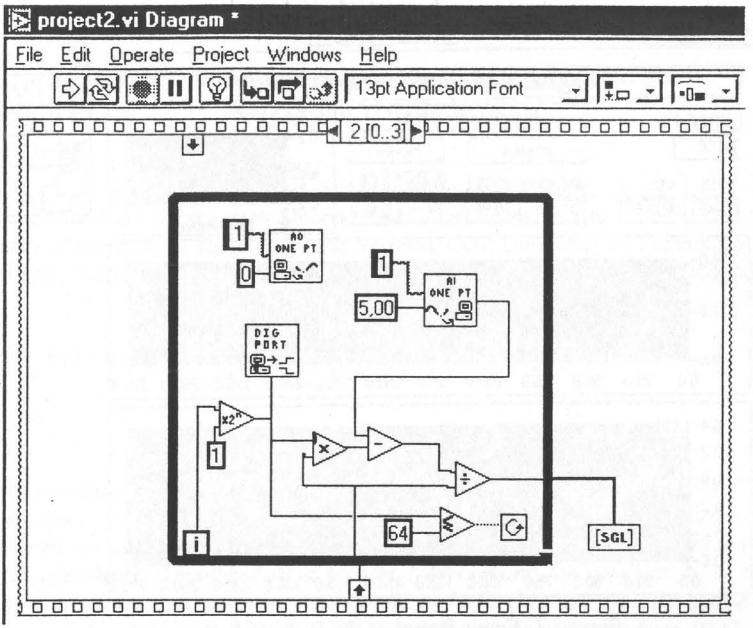


Figure *5. Sequence 2 of the program*

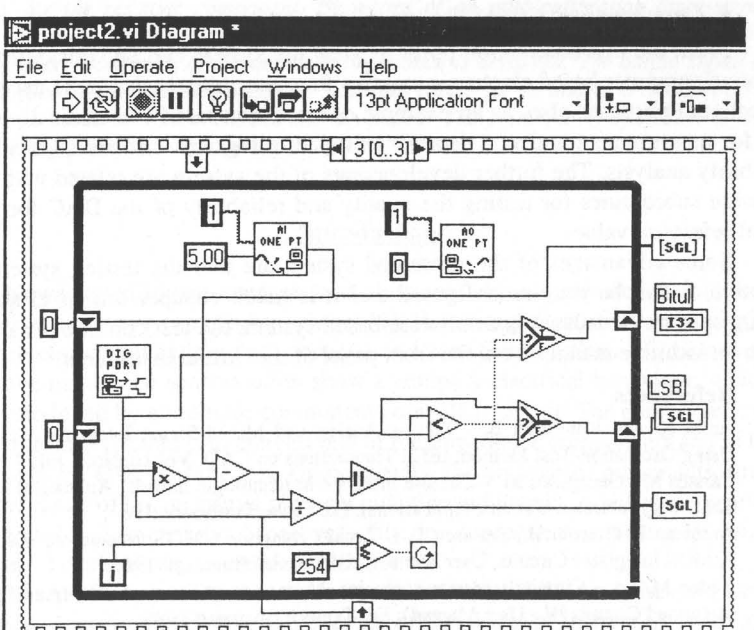


Figure *6. Sequence 3 of the program*

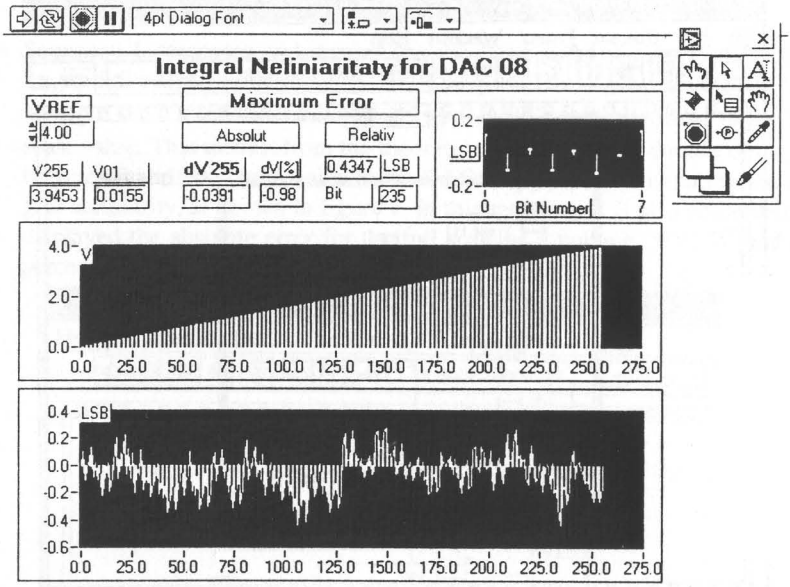


Figure 7. *Front Panel of the Virtual Instrument*

5. Conclusions

From the instrumentation point of view the system can be considered an adaptive computer based electronic systems for measurement. It can be used for educational purposes also, as an example of computer based electronically system for measurement and as a data generator for integrated circuits quality and reliability analysis. The further developments of the system are related with the software subroutines for testing the quality and reliability of the DAC for different reference values.

Some advantages of the presented system are that the testing system is adaptive, it can be easy reconfigured and it is much cheaper than a classical testing system. Because it is a software-based system, the test conditions can be set in an intuitive manner from the front panel of the virtual instrument.

References

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