Stress sensors based on the use of the piezojunction effect

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Abstract: *Due to the piezojunction effect, the* $I_C(V_{BE})$ *characteristics of bipolar transistors are affected by mechanical stress. Therefore, this effect is the dominant source of inaccuracy of many analogue circuits, such as smart temperature sensors and bandgap references. On the other hand, the effect can also be used in new mechanical sensors. This paper shows how to minimize or to maximize the influence of the piezojunction effect of PNP lateral transistors on [100] silicon. A novel current mirror design, which is suitable to be used as a stress sensor, is presented. As compared to sensors based on the piezoresistive effect, the new sensor offers the advantage that it is very small and has a reduced power consumption. The current mirror gauge factor amounts to 176; the nonlinearity is less than ±1% and the temperature coefficient of the gauge factor is* $1.75\times10^{-3}\,{}^{o}C^{-1}$.

Keywords: piezojunction effect, current-mode stress sensor, lateral transistor

Introduction

Usually, bipolar IC processes are designed to optimize the performance of vertical NPN (V-NPN) transistors. In order to expand the VLSI design capabilities, a lateral PNP (L-PNP) transistor is available. However this transistor is often considered as a poor device with inferior performance as compared to that of the V-NPN. In a previous paper [1] we presented experimental results for the piezojunction effect in the V-NPN. The maximal relative variation in the saturation current was found to be approximately 6% for a stress of 140 MPa.

This paper shows how the L-PNP can be used to take advantage of the anisotropic behavior of the piezojunction effect. In this device the main current flow is lateral and the designer has the freedom to choose the current direction in relation to the wafer crystal orientation. This option is not available in the V-NPN. Using an appropriate layout, one can minimize the piezojunction effect in L-PNPs on a [100] oriented silicon wafer. The piezojunction effect can be maximized using a current mirror with orthogonal aligned L-PNP transistors. Such a device is very suitable for the function of stress sensor. This new sensor based on the piezojunction effect is small compared to the stress sensor based on the piezoresistive effect, which requires a large area because of the low sheet resistance provided by the IC technology. Other advantages are the lower power consumption, which is an important feature for battery-operated sensors, and the current mode output signal, which can easily be processed.

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Piezojunction effect

The piezojunction effect is the mechanical-stress-induced change of the bipolar transistor saturation current. The saturation current is approximated by:

$$I_0 = A_E \frac{kT}{Q_B} \mu n_i^2, \qquad (1)$$

where A_E is the emitter area, k is the Boltzmann constant, T the temperature, Q_B the Gummel number, μ the minority-carrier mobility in the base and n_i the intrinsic carrier concentration. At a stress lower than 200 MPa, the geometrical deformations in A_E and Q_B are so small that they can be ignored [2]. On the other hand, the stress-induced changes in both μ and n_i^2 can modify I_0 considerably. The stress-induced change in the I_0 can be approximated by a superposition of two relative variations:

$$\frac{\Delta I_0}{I_0} \cong \frac{\Delta n_i^2}{n_i^2} + \frac{\Delta \mu}{\mu}. \qquad (2)$$

The Δn_i^2 variation is due to the band-edge shifts. This variation depends on the stress orientation, but not on the current direction related to the silicon crystal orientation [3]. The $\Delta\mu$ variation concerns the minority-carrier mobility in the base. We assume that μ varies linearly with mechanical stress [4]. Using the established piezoresistivity theory, the relative mobility change for an arbitrary oriented lateral transistor on [100] silicon wafer can be calculated from:

$$\begin{aligned}\frac{\Delta\mu}{\mu} = \sigma\Bigg[&\pi_{44}\left(\frac{1}{2}\sin 2\varphi \sin 2\lambda\right) \\ &+\pi_{12}\left(\frac{1}{2}-\frac{1}{2}\cos 2\varphi \cos 2\lambda\right) \\ &+\pi_{11}\left(\frac{1}{2}+\frac{1}{2}\cos 2\varphi \cos 2\lambda\right)\Bigg]\end{aligned} \qquad (3)$$

where σ and λ represent the amount and the direction of the stress, respectively; φ is the direction of the current and π_{11}, π_{12} and π_{44} are the independent piezoresistive coefficients for the minority carrier mobility in the base. The in-plane directions λ and φ are considered with respect to the silicon wafer axis [100]. The value of π_{44} amounts to 9.56×10^{-10} Pa^{-1} and it appears to be much larger than that of π_{11} and π_{12} [5].

L-PNP transistor on [100] silicon

The L-PNP transistors are fabricated in a conventional bipolar process. They are implemented using a p-diffusion in the epitaxial layer (base) as the emitter and a second p-diffusion for the collector. An n+ buried layer is formed to prevent the collection of carriers in the p-substrate. The transistor action takes place laterally. If the transistors are designed as a finger structure, where the collector runs in parallel with the emitter, most of the carriers injected from the emitter flow in a preferential direction, reaching the collector laterally. If we consider two orthogonal transistors with a current-flow direction of φ and $\varphi+\pi/2$, the stress-induced change in mobility due to π_{44} can be calculated based on Equation 3. Figure 1 shows the result versus the stress direction λ in the wafer plane.

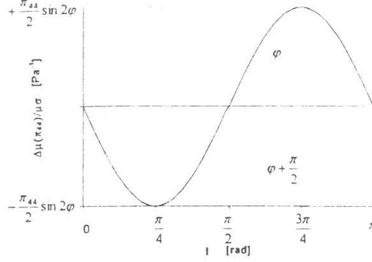

Fig. 1: Stress-induced change in μ due to π_{44} for two orthogonal current directions.

This figure shows that the maximum value of the stress-induced change in μ appears for $\lambda=\pi/4$ or $\lambda=3\pi/4$. The magnitude of the maximum depends on φ. In order to maximize the anisotropic effect due to π_{44}, we chose the orientations $\lambda=3\pi/4$ and $\varphi=\pi/4$.
Figure 2 shows the layout of the L-PNP transistors and the wafer crystal orientation. The transistors $Q_{\pi/4}$, $Q_{3\pi/4}$, $Q_{-3\pi/4}$ and $Q_{-\pi/4}$ form a common centroid geometry. They were designed as a finger structure with an emitter area of A_E= 86μm × 6μm. In each transistor the current flows in a different direction, which is given by its index.
The stress-induced changes in μ amount to:

$$\frac{\Delta\mu}{\mu\sigma}=\frac{\pm\pi_{44}-\pi_{12}-\pi_{11}}{2}. \quad (4)$$

The sign of the coefficient π_{44} depends on the direction of the transistor current. It is positive for $Q_{3\pi/4}$, or $Q_{-\pi/4}$, and negative for $Q_{\pi/4}$, or $Q_{-3\pi/4}$ [5].

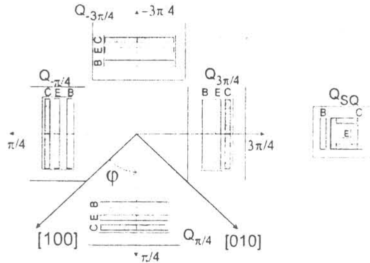

Fig.2: Layout of the L-PNP transistors on a [100] silicon wafer.

The transistor Q_{SQ} shown in Figure 2 minimizes the stress effect. It has a square emitter, A_E=8 μm × 8 μm, surrounded by a square collector. This layout minimizes the stress-induced change in μ by compensating of the coefficient π_{44}, because the same number of carriers flow in each orthogonal direction. Thus, the remaining stress effect in the I_0 is mainly due to the stress induced change in n_i^2.

Stress sensing circuit

The connection of two orthogonal transistor pairs, operated as current mirror, form a matched temperature-compensated circuit with a high sensitivity for mechanical stress.

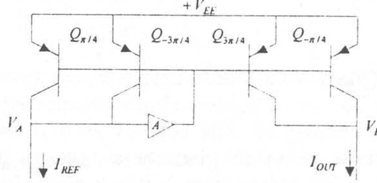

Fig. 3: Current mirror as a current-mode stress sensor.

In our experimental setup the off-chip amplifier A is introduced to reduce the influence of the base currents. To reduce the influence of the Early effect on the mirror ratio, we determined the voltage V_B by means of an external circuit, so that $V_A=V_B$. If we consider the stress-induced change in μ and n_i^2, the mirror ratio m can be described by:

$$m=\frac{I_{OUT}}{I_{REF}}=\frac{I_{03\pi/4}}{I_{0\pi/4}}=\frac{I_{0-\pi/4}}{I_{0-3\pi/4}}=\frac{[(\mu+\Delta\mu)(n_i^2+\Delta n_i^2)]_{3\pi/4}}{[(\mu+\Delta\mu)(n_i^2+\Delta n_i^2)]_{\pi/4}} \qquad (5)$$

where all variations are stress dependent. The Δn_i^2 does not depend on the current direction, so this effect is cancelled. Based on the equations 4 and 5, the mirror ratio can be simplified to:

$$m=\frac{\left(\frac{+\pi_{44}-\pi_{12}-\pi_{11}}{2}\right)\sigma+1}{\left(\frac{-\pi_{44}-\pi_{12}-\pi_{11}}{2}\right)\sigma+1}. \qquad (6)$$

Next, m can be approximated by a second-order Taylor series:

$$m=\left(1+\pi_{44}\sigma-\pi_{44}\left(\frac{-\pi_{44}-\pi_{12}-\pi_{11}}{2}\right)\sigma^2\right). \qquad (7)$$

This equation represents the theoretical stress-induced change of the mirror ratio of the current mirror formed by two orthogonal L-PNP transistors, where the stress and current direction are equal to $\lambda=3\pi/4$ and $\varphi=\pi/4$, respectively.

Experimental result

The transistors have been tested at a room temperature of 25 °C using a special apparatus that applies the principle of the cantilever technique [1]. Figure 4 shows a marked influence of the current direction on the stress-induced relative variation in I_0, where $I_{0\sigma}$ is the stressed I_0.

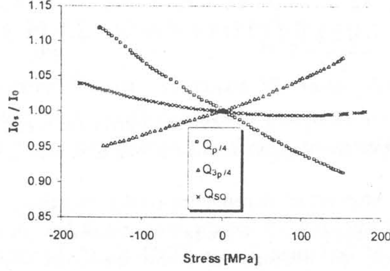

Fig. 4: Measured variation in I_0 for L-PNP with different current directions.

Basically, this result reflects the very high anisotropy due to the coefficient π_{44} for minority carrier concentration. All curves show quadratic behavior due to the influence of n_i^2. The transistor Q_{SQ} has the lowest stress sensitivity due to the compensation of π_{44}.

The current mirror formed by orthogonal transistors was tested at room temperature. Figure 5 shows the mirror ratio versus stress, where I_{REF}=10 μA. The theoretical curve was calculated using the Equation 7 for π_{44}=9.56×10^{-10} Pa^{-1}. We neglected π_{11} and π_{12} because they are much smaller than π_{44}.

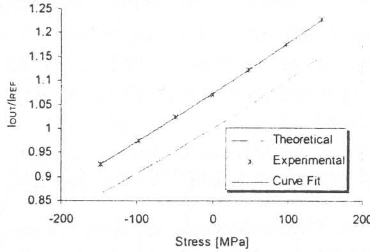

Fig. 5: Measured mirror ratio versus applied stress.

Using a second-order curve fit of the experimental result, we obtain the equation:

$$m = a_0 + a_1\sigma + a_2\sigma^2, \qquad (8)$$

with a_0=1.07, a_1=1.03×10^{-9} Pa^{-1} and a_2=2.37×10^{-19} Pa^{-2}.

The experimental result presents an initial offset of 7% caused by the transistor mismatching, which is not predicted by theory. This offset is due to the stress induced by wafer fabrication, the mismatching in the emitter areas and the doping spread. The experimental first-order stress dependence a_1 is in accordance with Equation 7. The main part of the second-order coefficient a_2 is also predicted by Equation 7. The nonlinearity appears to be less than ±1% for the stress range from −150MPa to +150MPa.

The gauge factor is one of the most important characteristics to consider for strain/stress sensors. The definition of the current mirror gauge factor is similar to that used in piezoresistivity theory. It is a dimensionless quantity representing the relative

change of the mirror ratio per unit strain. The gauge factor K at a temperature of 25 °C can be calculated by:

$$K = \frac{\Delta m \; m_0}{\sigma \; E} = 176, \qquad (9)$$

where $\Delta m/m_0$ is the relative change of the current mirror ratio and E is the Young's modulus in the direction of the applied strain. In our case, for $\lambda=\pi/4$, it holds that E=170.7 GPa. [6]
The measurement of the temperature dependence of the sensitivity was performed by placing the devices under test (DUT) inside an oven. It has been found that the Temperature Coefficient of the Gauge Factor TCGF=-1.75×10^{-3} $^{o}C^{-1}$ [7].

Discussion and Conclusion

A new stress-sensing circuit using L-PNP transistors on [100] silicon, which is based on the piezojunction effect, has been designed and tested. The linearity, gauge factor and the temperature coefficient of the gauge factor are approximately the same as those of the sensors based on the piezoresistive effect, which are widely used to measure strain, stress, pressure and acceleration. Some advantages of the stress sensor based on the piezojunction effect over the sensor based on the piezoresistive effect are a lower power consumption and the reduced size occupied by the layout. Furthermore, this sensor has a current-mode output signal which can easily be processed. We have also shown that using a common square-emitter layout geometry minimizes the piezojunction effect.

References

[1] F. Fruett and G.C.M. Meijer 'A test structure to characterize the piezojunction effect and its influence on silicon temperature sensors', Eurosensors XIII, The Netherlands, 1999, pp. 23-24

[2] H. Mikoshiba and Y. Tomita, 'Piezoresistence as the source of stress-induced change of current gain in bipolar transiistors', Solid-State Electronics, 1982, Vol.25, no3, pp. 197-199

[3] J.F. Creemer and P.J. French 'Theoretical and experimental study of the piezojunction effect in bipolar transistors under moderate stress levels', Digest of technical papers, Transducers'99, Sendai, Japan, June 7-10, 1999, pp. 204-208

[4] C. S. Smith, 'Piezoresistance effect in germanium and silicon' Phys. Rev., vol. 94, 1954, pp. 42.49

[5] F. Fruett and G.C.M. Meijer, 'Measurement and compensation of piezoresistive coefficient π_{44} for minority-carrier concentration', Electron. Lett., 2000, 36, (2), pp. 173-174

[6] J.J. Wortman and R.A. Evans, 'Young's modulus, shear modulus, and poisson's ratio in silicon and germanium', Journal of applied physics, 1965, 36, (1), pp. 153-156

[7] F. Fruett and G.C.M. Meijer, "Exploration of the piezojunction effect using PNP lateral transistors on (100) silicon" Eurosensors XIV, Copenhagen, Denmark, Aug. 2000