AN ECL CIRCUIT WITH SYMETRICAL CAPACITANCE-COUPLED ACTIVE PULL-DOWN EMITTER FOLLOWER STAGES

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Abstract

An ECL circuit with symmetrical capacitance-coupled active pull-down emitter follower stages is described. The speed-up effect is achieved by the cross-coupling of two reverse connected diodes, which are used as capacitors. The circuit can operate at a higher speed with smaller power dissipation than the conventional ECL gate. In contrast to many active pull-down ECL circuits it has differential outputs. This circuit is capable of providing the logic functions of conventional ECL gate excepting wired-OR and is independent of the supply voltage. It can be used in symmetrical differential stages operating as gates, high-speed comparators etc. Since the emitter followers are supplied from a current mirror, the power consumption can be controlled according to the desired speed. The circuit can be implemented in a standard bipolar technology and do not require additional supply voltages. Simulation results proving predicted circuit behavior are demonstrated and a comparison with other active pull-down ECL circuits is made. The circuit efficacy is examined at different loads.

1. INTRODUCTION

Compared to the conventional ECL gate, the active pull-down ECL (APD-ECL) circuits improve the fall time of the output voltage and the power dissipation. The APD-ECL circuits are two kinds. In the circuits of the first kind, one of which is shown in Fig.1 [1], static current is used to discharge the load capacitance.

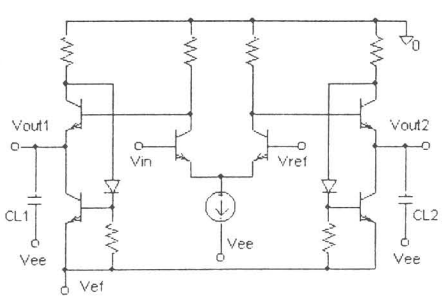

Fig.1 FDP-EF-ECL circuit

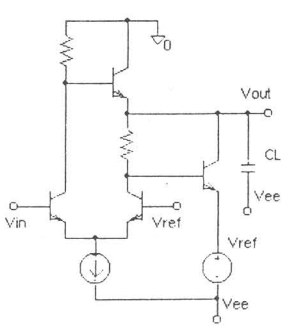

Fig.2 LS-APD-ECL circuit

Hence these circuits are not able to significantly reduce the power dissipation. In the circuits of the second kind a dynamic current discharges the load capacitance. So the

static current and therefore the power dissipation can be significantly reduced. These circuits are with self-adjusting driving capability, or with a capacitor. LS-APD-ECL circuit [2], depicted in Fig.2, is the best of the circuits with self-adjusting driving capability. It has very good properties, but it has not differential outputs. There are many APD-ECL circuits with a capacitor, to which belongs the proposed circuit. AC-coupled APD-ECL circuit [3] and CB-APD-ECL circuit [4], shown in Fig.3, have only an inversion output and moreover they have certain drawbacks. In AC-coupled APD-ECL circuit the current through the speed-up capacitor Cx is limited by the collector resistor.

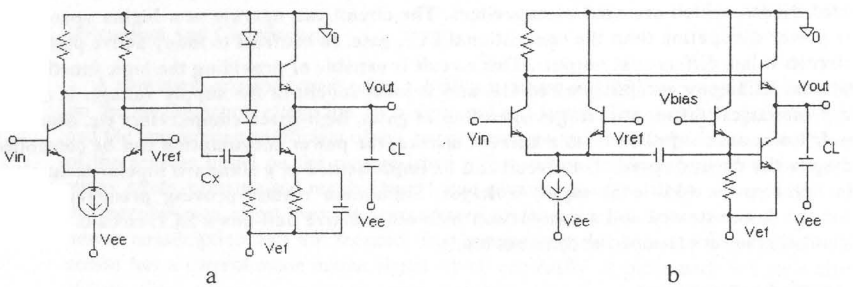

Fig.3 (a) AC-coupled APD-ECL circuit; (b) CB-APD-ECL circuit

CB-APD-ECL circuit is inapplicable in some two-level schemes, for example XOR. FCCS-APD-ECL circuit [5], depicted in Fig.4, shows very good results, but it is very sensitive to the value of supply voltage. Four emitter followers are necessary in this circuit to obtain differential outputs and it does not allow wired-OR.

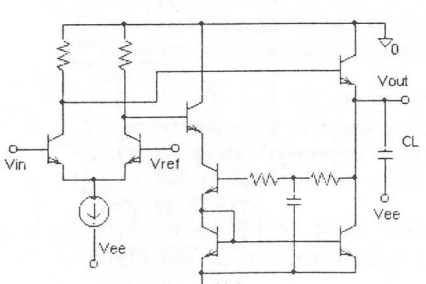

Fig.4 FCCS-APD-ECL circuit

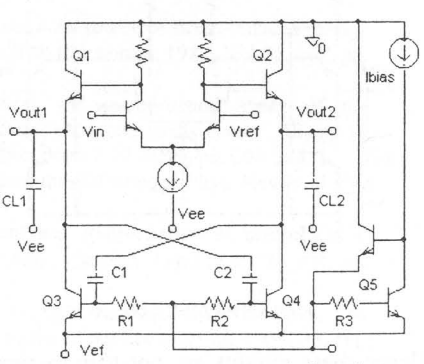

Fig.5 The proposed circuit

2. CIRCUIT OPERATION

The proposed circuit is shown in Fig.5. Its operation is independent of the supply voltage Vef, which can be with a minimal value. CL1 and CL2 are load capacitance, R1=R2=R3 and C1=C2. When the input voltage Vin is "low", the outputs Vout1 and Vout2 are accordingly "high" and "low". The currents through Q1, Q2, Q3, Q4 and Q5 are equal to Ibias. When Vin goes from "low" to "high", the voltage at the base of Q2 rises and the current through Q2 charges CL2 to "high". C1 transmits the rise of Vout2 to the base of Q3, the current through Q3 increases and Vout1 falls quickly. The increase of current through Q3 depends on the ratio between C1 and the input capacitance of Q3. The time in which this current falls to Ibias depends on the time constant R1C1.

Because of the cross-coupling, wired-OR is possible only between gates, whose noninversion output is not used [6]. Such circuit is shown in Fig.6.

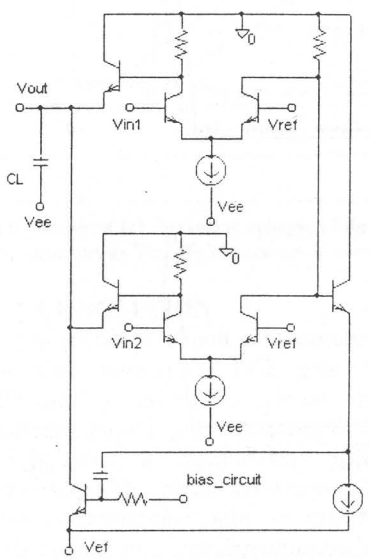

Fig.6 A two input wired-OR

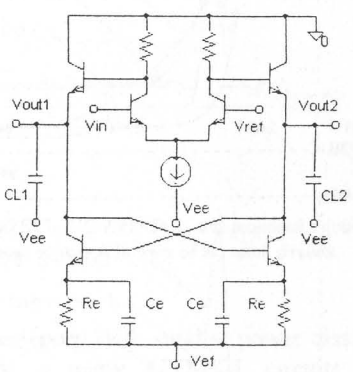

Fig.7 CC-APD-ECL circuit

3. SIMULATION RESULTS

The proposed circuit operation is compared with that of the conventional ECL gate and with the operation of the cross-coupled active pull-down ECL (CC-APD-ECL) circuit [6], shown in Fig.7. CC-APD-ECL circuit is very simple and requires no extra biasing circuit, but its minimal supply voltage Vef is higher than that of the proposed

circuit. Moreover the current consumption of the CC-APD-ECL circuit is very sensitive to the value of supply voltage. The output voltages and the current consumption of the emitter followers of the conventional ECL, CC-APD-ECL and the proposed circuit at the same pulse input voltage are depicted in Fig.8. and Fig.9 accordingly with fan-out=1 and 4. Transistors DMRF9331 are used in all simulated circuits, whose main parameters are:

Bf=230, Vaf=44V, Rb=54Ω, Re=1Ω, Cje=100fF, Cjc=160fF, tf=13ps.

In the CC-APD-ECL circuit Vef=-2.1V, Re=4kΩ, so the ratio between static current through the emitter followers is five [6] and the speed-up capacitors Ce are 0.8pf. In the proposed circuit Vef=-1.8V, a reverse connected diode (transistor connected as a diode) serves as a capacitor C1 and R1=1.5kΩ.

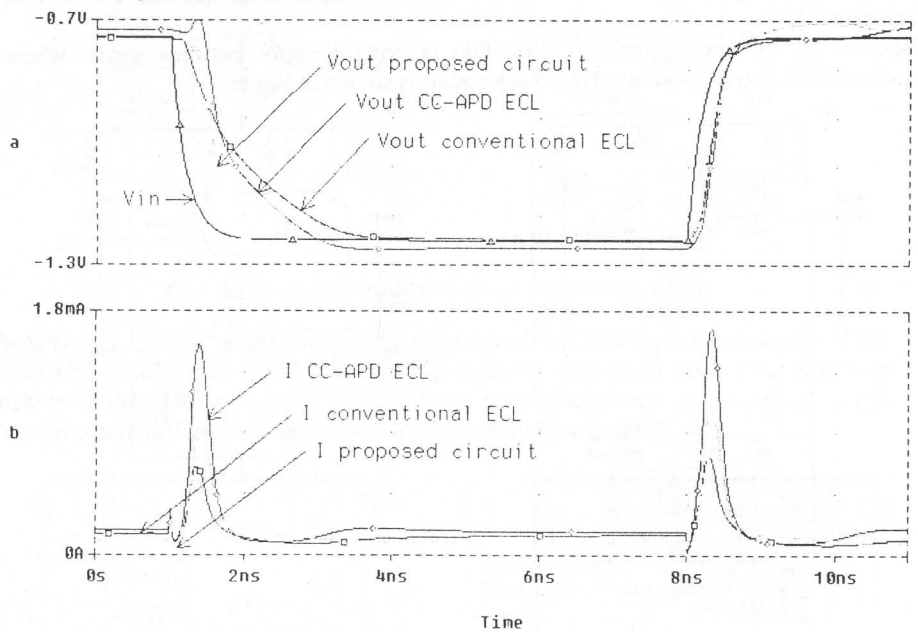

Fig.8 *fan-out=1* (a) The output voltages of the conventional ECL, CC-APD-ECL and proposed circuit for the same input voltage Vin.; (b) The consumed current of the output emitter followers of the same circuits.

It can be seen that the proposed circuit has a big load capability with very small speed-up capacitors. In spite of its lower power consumption and much smaller speed-up capacitors, the proposed circuit surpasses the CC-APD-ECL circuit.

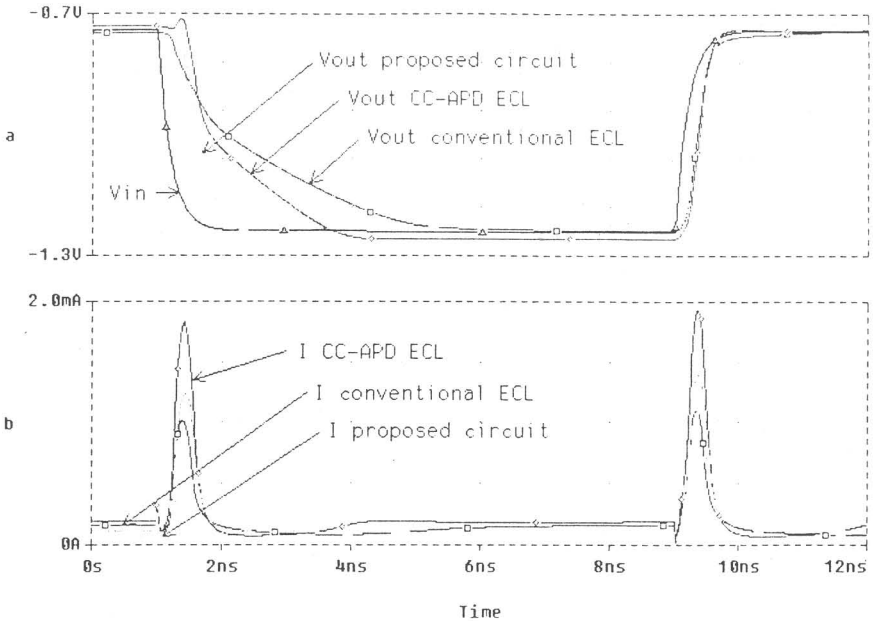

Fig.9 ***fan-out=4*** (a) The output voltages of the conventional ECL, CC-APD-ECL and proposed circuit for the same input voltage Vin.; (b) The consumed current of the output emitter followers of the same circuits.

4. CONCLUSION

The proposed circuit can operate at a higher speed with smaller power dissipation than the conventional ECL gate. In contrast to many APD-ECL circuits it has differential outputs. The circuit is capable of providing the logic functions of conventional ECL gate excepting wired-OR and is independent of the supply voltage. It can be used in symmetrical differential stages operating as gates, high-speed comparators etc. Since the emitter followers are supplied from a current mirror, the power consumption can be controlled according to the desired speed. The circuit can be implemented in a standard bipolar technology and do not require additional supply voltages.

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