Simple Static Induction Thyristor Model for PSpice Simulation

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Abstract: *A simple PSpice model for the static induction thyristor (SITh) is proposed. The proposed model is based on the SITh's static and dynamic behaviour. The simulated static and switching characteristics correspond well to the experimental results given in [1]. The model has passed all performed tests. Although the proposed model is not an ideal solution it will help to start simulating the circuits containing the static induction thyristors.*

Keywords: *PSpice, simulation, modeling, static induction thyristor, power semiconductor*

1. INTRODUCTION

A static induction thyristor (SITh) is a device in the static induction transistor (SIT) family. The SITh basic structure is consisted of a $p^+n^-n^+$ diode with the n^- region containing p gate regions. The schematic view of the SITh structure is shown in Fig. 1.

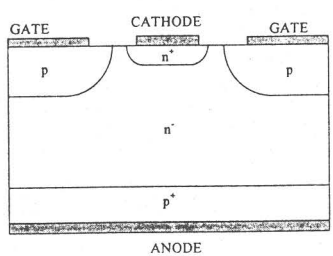


Fig. 1 *Schematic view of a SI thyristor*

The gate regions of the device are designed to pinch off the current path when a reverse bias voltage is applied between the gate and the cathode. When a reverse gate bias is not applied, the SITh behaves like conventional diode. The blocking voltage rating of an SI thyristor (or Field Controlled Thyristor) is more than 2000 volts and the average current rating is up to several hundreds of amperes (2500V/500A has been reported in [1]). The SI thyristor has several features useful in high power switching devices, such as high switching speed, high *dv/dt* and *di/dt* capabilities, low

forward voltage drop, and ability to operate at high temperatures. Up to now, there has not been reported any attempt for PSpice simulation of circuits containing static induction thyristors or PSpice models for the SITh. The purpose of this work is to propose a model suitable for computer analysis and simulation of circuits containing SIThs. The proposed model is based on the SITh's static and dynamic behaviour, and not on the physical structure of the device.

2. THE PSPICE MODEL FOR THE SI THYRISTOR

The circuit behavioral PSpice model for the SITh is shown in Fig. 2 and its subcircuit file is given in the appendix.

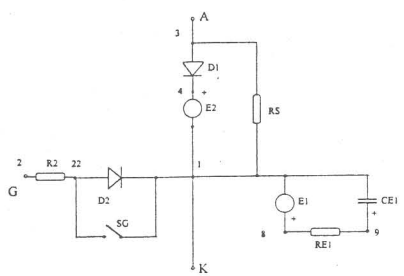


Fig. 2. *PSpice model of the SITh*

The main current path is consisted of the diode D_1 and the voltage controlled voltage source (VCVS) E_2. The diode D_1 provides the forward conducting and the reverse blocking characteristics of the device. The VCVS E_2 is used to implement the forward blocking capabilities of the model with the appropriate gain and delay time. Its voltage depends on the gate voltage and on the $R_{E1}C_{E1}$ time constant. The forward blocking voltage depends on the VCVS E_2 and can be calculated as:

$$V_{BR,AK} \approx |V_{GK}| \cdot p \cdot \frac{q + |V_{GK}|}{r} \cdot 1.5 \qquad (1)$$

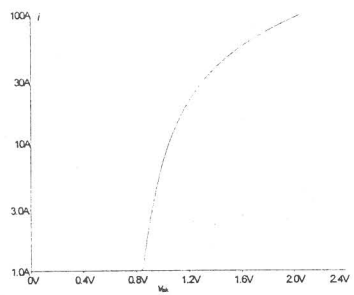
where p, q and r are parameters which can be obtained by simple measurements of three curves in the family of the forward blocking characteristics for the value of the current of 2mA. For our simulations we have obtained: p=8, q=40V and r=30.

The gate circuit is consisted of the diode D_2, resistor R_2 and the voltage controlled switch S_G. The diode D_2 is used to simulate the pn junction nature of the gate and the switch S_G is there to speed up the discharging process of the capacitor.

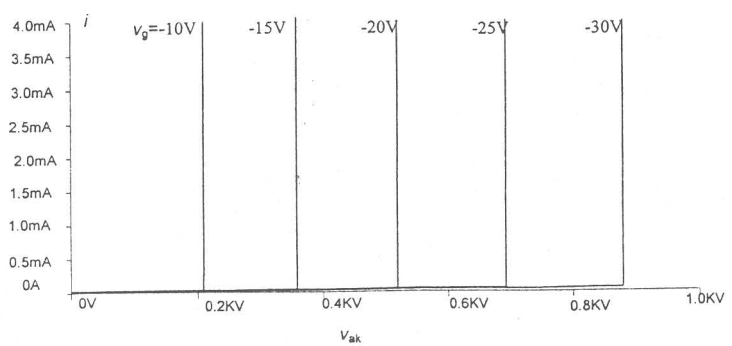
The operation of the model is as follows: when the gate to cathode voltage is zero the SITh is working as a diode allowing the current in the forward direction and blocking the current in the reverse direction. The reverse breakdown is determined by the reverse breakdown voltage of the diode D_1. When the reverse voltage is applied between the gate and cathode the device is starting to block the current in the forward direction up to the voltage defined by (1).

3. SIMULATION RESULTS

Extensive simulations have been performed in order to test the proposed model characteristics. The model has passed all performed tests and can be used to analyze various types of power converters using SI thyristors.



(a)

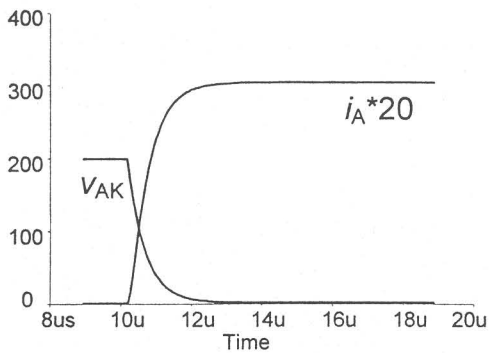


(b)

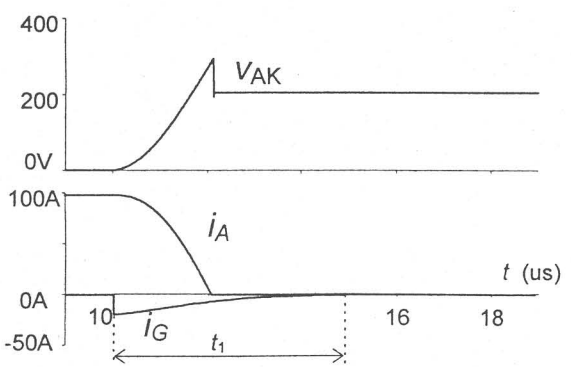
Fig. 3. *Static I-V characteristic of the PSpice model for the SITh given in Fig. 1 a) forward conducting state; b) forward blocking state*

The simulated static characteristics during the forward conduction and forward blocking state are shown in Fig. 3-(a and b). They correspond well with those presented in [1].

The switching waveforms during the turn-on and turn-off are simulated according to Terasawa [1] and the obtained results are shown in Fig. 4. Comparing with the measured results given in [1] it can be seen that all phenomena observed during the switching process are obtained also by simulation. We can point out the appearance of the overvoltage and the $i_G(t)$ characteristics shown in Fig. 4-b.



(a)



(b)

Fig. 4. *Switching characteristics of the PSpice model for the SITh given in Fig. 1: a) during turn-on; (b) during turn-off*

The shape of the $i_G(t)$ is not an exact copy of the corresponding characteristic shown in [1]. The better correspondence is obtained using a small inductance (0.5 μH) in the gate circuit.

4. CONCLUSION

A simple PSpice model for the static induction thyristor is proposed. The model is based on the device behaviour rather than on the physical structure of the SITh. Simple equation for determining some of the model parameters has been given. Extensive simulations have been performed to examine the model characteristics. The model has passed all performed tests and the results correspond very well with the experimental ones given in [1]. Although the proposed model is not an ideal solution it will help to start simulating the circuits containing the static induction thyristor.

5. REFERENCES:

[1] Y. Terasawa and M. Okamura" High Power Static Induction Thyristor", in *Semi-conductor Technologies*, editor J. Nishizawa, North-Holland, 1982, pp 241-248

APPENDIX

Subcircuit definition of the SI Thyristor model from Fig. 2

```
.subckt sith   3   2   1
*--------------A   G   K
d1 3 4 d1
.model d1 d(rs=.01 is=1e-7 n=2)
e2 1 4 9 1 1.5
d2 22 1 d2
sg 22 1 1 2 s1
.model s1 vswitch(ron=.001 roff=1e6 von=0 voff=.1)
r2 2 22 1
.model d2 d(cjo=5u rs=.02 is=1e-6)
e1 8 1 value = {((v(22,1)*8)*((40-v(22,1))/30))}
re1 8 9 1
ce1 9 1 .5u
rs 3 1 24meg
.ends
```