12V-to-15V PWM-Regulated Switched-Capacitor DC-to-DC Voltage Converter

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Summary *- A practical solution for obtaining PWM-regulated 15V output DC voltage from 12V DC input voltage with high efficiency inductorless circuit is proposed. Two configurations are pointed out: the minimum component count configuration, and the low output voltage ripple configuration. Rough design equations are derived and component values are calculated. The characteristics of the converters are investigated and compared using PSPICE simulation with standard models for power MOS switches and proven model for the switch driver [1]. The results show good performances at wide load and input-voltage variations.*

I. INTRODUCTION

Switched capacitor circuits have been known for a long period of time in electronics, starting from AC/DC voltage doublers and multipliers. There are articles that represent switched-capacitor DC-to-DC voltage converters as DC-to-DC voltage transformers utilizing output-to-input voltage transformation ratio equal to a whole number (step-up transformation) or inverse of a whole number (step-down transformation) [2]. Many articles have appeared recently treating PWM controlled switched-capacitor DC-to-DC voltage converters [3, 4], but they also utilize output-to-input voltage transformation ratio equal to a whole number or inverse of a whole number. Main characteristics of these circuits are low electromagnetic radiation, high efficiency and possible integrated circuit realization.

If low difference input-to-output voltage transformation is needed (such as 12V-to-15V) these circuits fail in efficiency. For example, if a voltage doubler is used and linear or PWM regulation of the output voltage is implemented, the efficiency drops down to 50% (even if the problem with extremely low duty ratios needed for PWM control is neglected).

A topological solution for fractional voltage ratios is given in [5], but no practical circuits have been reported. This article proposes two circuits:

1. the minimum component count (basic) converter - that corresponds to the idea in [5],
2. the modified basic converter with increased component count but reduced output voltage ripple.

II. THE MINIMUM COMPONENT COUNT (BASIC) CONVERTER

Fig.1 shows the basic converter circuit diagram (without the parasitic resistances of the capacitors) and Fig.2 shows the switch driving waveforms. The converter operates in two phases determined by the switch M_1 states: M_1-OFF and M_1-ON. Switch M_2 turns ON during the OFF-phase and connects capacitors C_1 and C_2 in series through diodes D_1 and D_2 to the input voltage source V_I (Fig. 3). The duration of the capacitor charging is determined by the duty factor d. During the ON-phase the capacitors C_1 and C_2 are connected in parallel through diodes D_3, D_4 and D_5 and are discharged into the output capacitor C_3 through the switch M_1 and the input voltage source V_I (Fig. 4).

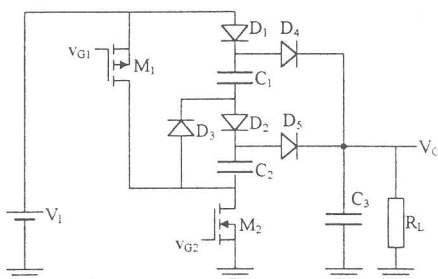

Fig. 1. The Basic 12V-to-15V Converter Circuit Diagram

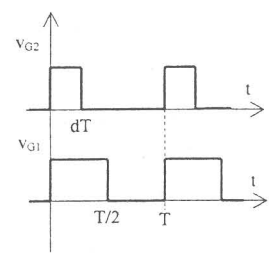

Fig. 2 . Switch Driving Waveforms

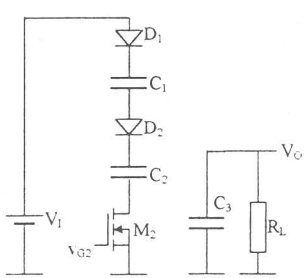

Fig. 3. The Converter in Phase OFF

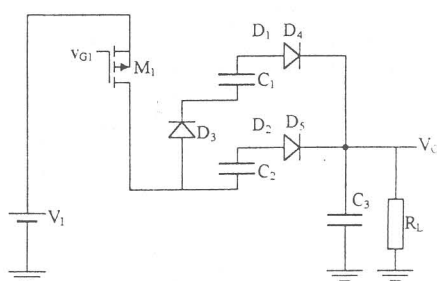

Fig. 4. The Converter in Phase ON

We can notice a little misbalance in the voltages of the two switched capacitors C_1 and C_2 because of the two diodes in series with C_1 in phase ON, but it does not affect the operation of the converter. Since C_1 and C_2 can be charged up to approximately $V_I/2$, the maximum no-load output voltage can be $3V_I/2$. By PWM

modulation of the charging interval (based on component series resistances), lower output voltages can be obtained and kept constant at load and input voltage variation.

II. THE MODIFIED CONVERTER (WITH REDUCED OUTPUT VOLTAGE RIPPLE)

The OFF-state of the basic converter is it's main disadvantage since the load is powered only by the output capacitor, while in the ON-state all three capacitors appear connected in parallel to the load. This asymmetry is a source of higher output voltage ripple. A circuit that would provide equal output capacitance in both states would also have lower output voltage ripple (at the same load). The most obvious solution is to use two sections of switched capacitors (Fig. 5) with switch driving voltages as shown in Fig. 6.

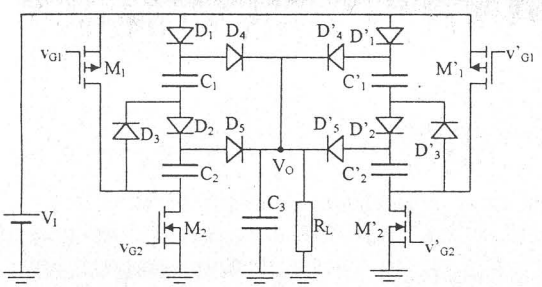

Fig. 5. The Modified Converter Circuit Diagram

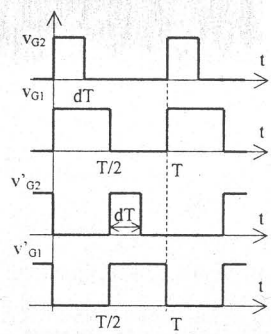

Fig. 6. Switch Driving Waveforms

In this converter phases ON and OFF actually does not exist but two actions appear at same time: charging of the capacitors of the "left group" while discharging the capacitors of the "right group" (denoted by apostrophe) in the first half-cycle, and vice-versa in the second half-cycle.

III. SOME DESIGN CONSIDERATIONS

If a converter is to be designed one has to have some idea about the component values in order to achieve certain converter characteristics. Therefore in this section a partial analysis of the charging and discharging processes within the basic converter is performed and rough design equations are derived.

In the OFF-state the equivalent circuit of the converter is as shown in Fig. 7. The main assumptions are:

$$C_1 = C_2 = C,\ C_3 = mC \quad ;\quad R_1 = R_2 = R,\ R_3 = R/m \quad ,$$

where m is a positive real number, and

$$R_L >> R_3 = R/m \ ,$$

so that R/m is removed from the discharging circuit at the output.

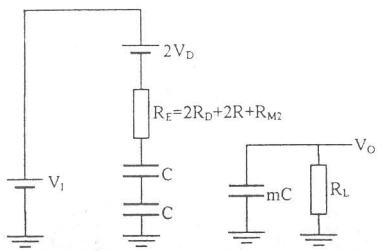

Fig. 7. OFF-state equivalent circuit

If the average value of the output voltage is V_O , it can be used as approximate initial value for $v_O(t)$ during OFF-phase:

$$v_O(t) = V_O(1 - e^{-\frac{t}{\tau_{dis}}}) \ .$$

Since $\tau_{dis} >> T/2$ we can write:

$$v_O(\tfrac{T}{2}) \approx V_O(1 - \frac{T}{2\tau_{dis}}) = V_{O\min} \ ,$$

and the output voltage ripple can be approximated with

$$Vr \approx 2(V_O - V_{O\min}) = V_O \frac{T}{\tau_{dis}} \ .$$

To obtain the desired relative output voltage ripple V_r/V_O, the switching period T must satisfy the relation:

$$\frac{T}{\tau_{dis}} \le \frac{Vr}{V_O} \ . \qquad (1)$$

From the charging circuit at the input we obtain $\tau_{ch} = \frac{C}{2}(R_{M2} + 2R + 2R_D)$. Nearly full charging of the capacitors at maximum duty cycle $d=0.5$ can be obtained if $\tau_{ch} \le (T/2)/3$. Since voltage variations at the capacitors are small, the converter could operate down to input voltages little higher than $\frac{2}{3}V_O + 2V_D = 10.8V$. If the lowest input voltage is not lower than $11V$ then τ_{ch} can be little relaxed, so we can (arbitrarily) write:

$$\tau_{ch} \le \frac{T}{4} \ . \qquad (2)$$

If we chouse the switching frequency at $100kHz$, than $T=10\mu s$. Knowing the typical values of the resistances in the charging circuit: $R_{M2}=80m\Omega$ (IRF530), $R=20m\Omega$ (multilayer capacitors), $R_D=20m\Omega$ and $V_D=0.4V$ (1N5822), from (2) we obtain $C \le 31.3\mu F$ and decide $\boldsymbol{C=33\mu F}$. Putting $R_L=15\Omega$ ($I_L=1A$) and $V_r/V_O=1\%$, from (1) it follows: $\tau_{dis} \ge 100T \Rightarrow m \ge 100T/CR_L \Rightarrow \boldsymbol{m \ge 1}$.

IV. SIMULATION RESULTS

PSPICE models of the components from the previous section and the MOSFET driving subcircuit from [1] were used for simulation to investigate the necessary duty ratio d, output voltage ripple V_r and the efficiency η as functions of load variation and input voltage variation. The results are presented graphically in Fig. 8.

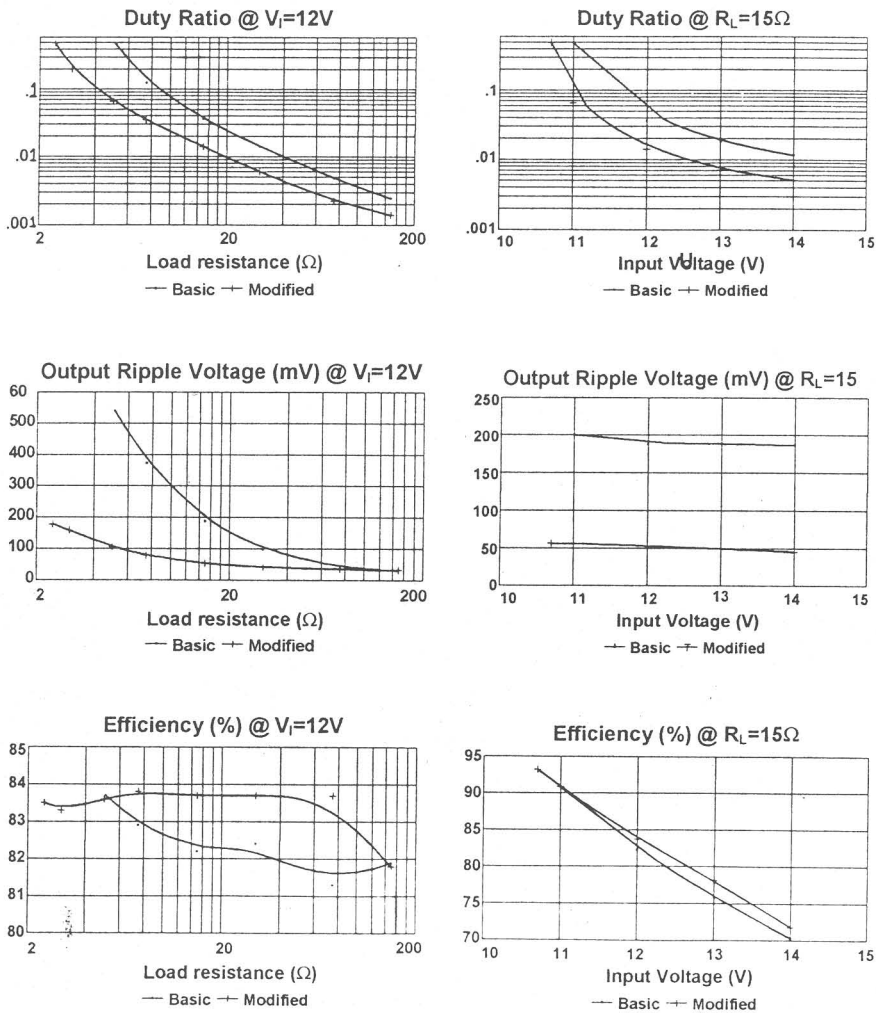

Fig. 8 Simulation Results

Diagrams show excellent efficiency at 12V input voltage for wide load variation and very good efficiency at rated load within the expected input voltage variation interval. The output voltage ripple at rated load and rated input voltage is a little higher than the expected by the design equations. This is mainly due to the neglected serial resistance of the output capacitance. The modified converter is obviously superior in output voltage ripple than the basic converter.

Duty ratio is generally very low which means that the capacitor charging can be further relaxed (probably at the expense of some small increase of the input voltage low limit). Extremely low duty cycles, that appear at higher input voltages and light loads, may become source of problems in practice.

IV. CONCLUSIONS

The converter presented in this article is a practical solution for fractional output-to-input conversion ratio applied in switched-capacitor PWM-controlled converters. Two configurations are proposed and investigated. Very rough design equations are derived and the calculated values are used for the converter simulation. The results show very good performances especially for the modified configuration.

Future work will be done to obtain better design equations, examine the dynamic performances of the converter and construct a prototype for experimental evaluation (preferably an IC type).

REFERENCES

[1] J. Kosev and G.L. Arsov, "12V to 5V Switched Capacitor DC-to-DC Converter with N-channel Power MOS Switches", in *ELECTRONICS '96 Conference Proceedings*, Sozopol, 1996

[2] Fumio Ueno, Takahiro Inoue, and Tohru Umeno, "Analysis and Application of Switched-Capacitor Transformers by Formulation", *Electronics and Communications in Japan, Part II: Electronics*, vol. 37, No.9, 1990, pp. 91-103

[3] S.V. Cheong, H. Chung, A. Ionovici, *Inductorless DC-to-DC Converter with High Power Density*, IEEE Transactions on Industrial Electronics, vol.41, No.2, APRIL 1994, pp. 208-215

[4] O. C. Mak, Y. C. Wong, and A. Ioinovici, "Step-up DC Power Supply Based on a Switched-Capacitor Circuit", in *IEEE Transactions on Industrial Electronics*, vol. 42, No.1, 1995, pp. 90-97

[5] M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC-DC converters", in *IEEE Power Electronics Specialists Conf. Rec.*, 1995, pp. 1215-1221