Features and limitations of CMOS Voltage References

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Abstract

This paper reviews the basic problems to be solved to enable the realisation of accurate voltage references in CMOS technology. These problems are due to the spreading in the characteristics of the reference elements, mismatching of components, 1/f noise, temperature effects and mechanical stress. It is shown that bipolar substrate transistors are very suited to be applied to generate the basic V_{BE} and PTAT voltages. Furthermore, it is shown that dynamic element matching and auto-calibration can solve the problems related to mismatching of components and 1/f noise. It is shown that mechanical stress is still a major source of inaccuracy. It is concluded that also with low-cost CMOS technology accurate voltage references and temperature sensors can be realised.

1. Introduction

Since their introduction in 1964 by Hilbiber [1] many types of bandgap-reference circuits have been presented. In [2] and [3] the principles and typical features of these circuits have been reviewed. Many of the presented circuits offer smart solutions to overcome the specific non-idealities of certain components or to optimise the behaviour for devices fabricated in a specific technology. It appears that in general the accuracy and long-term stability of CMOS bandgap voltage references are much less than that of bipolar ones. The low accuracy of the CMOS references is due to mismatching and drift of components, temperature effects, 1/f noise and mechanical stress. Recently [4] it has been shown that a major part of these problems can be solved by using chopped signals and by applying dynamic amplifiers and dividers. This paper reviews these novel dynamics signal-processing techniques. In case of an ideal signal processing of the basic signals, the accuracy is still limited by the accuracy of the basic signals themselves. In bandgap references the basic signals are: The base-emitter voltage V_{BE} of a bipolar substrate or lateral pnp transistor and the difference ΔV_{BE} of two of these base-emitter voltages, being a so-called PTAT voltage (PTAT = proportional to the absolute temperature). This paper presents novel results of an experimental and theoretical study of the accuracy of these basic signals for CMOS components.

2. Basic principles and device characterisation

2.1 Basic Principles

The principles of CMOS bandgap references are similar to those of bipolar ones. Figure 1 shows basic schematics of some conventional bandgap reference circuits implemented in bipolar and CMOS technology, respectively. In both circuits a compensating voltage $V_C(T)$ is added to $V_{BE}(T)$ to compensate for at least the first-order temperature dependence of $V_{BE}(T)$. This correction voltage is obtained by amplifying the difference $\Delta V_{BE} = (kT/q)\ln p$ of these base-emitter voltages of two

transistors operated at unequal collector-current densities with ratio p. In this way an output voltage V_{ref} is obtained for which it holds that:

$$V_{ref} = V_{BE}(T) + V_C(T) = V_{BE}(T) + A\Delta V_{BE}(T),$$ (1)

where A denotes an amplification factor.
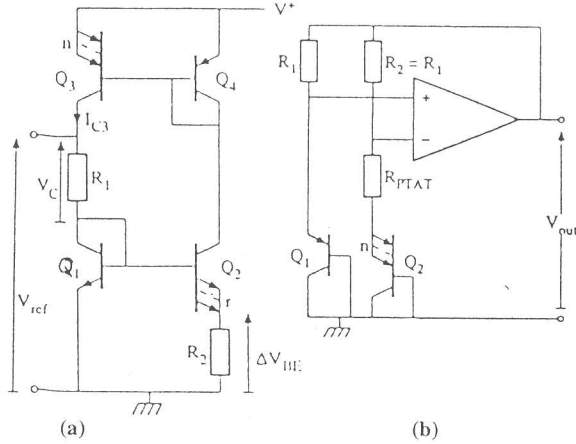

(a)   (b)

Fig. 1: Simple bandgap-reference circuits, implemented in (a) bipolar technology and (b) CMOS technology

In the circuit of Fig. 1(a) the action of the current mirror (Q_3, Q_4) ensures that the ratio of the collector currents of Q_1 and Q_2 remains constant. Neglecting the influence of the base currents and base-width modulation, for the voltage ΔV_{BE} across R_2 we find that:

$$\Delta V_{BE} = (kT/q)\ln(nr),$$ (2)

where r and n denote the saturation-current ratios I_{S2}/I_{S1} and I_{S3}/I_{S4} of (Q_2, Q_1) and (Q_3, Q_4), respectively. For the output voltage V_{ref} it holds that

$$V_{ref} = V_{BE1} + V_C = V_{BE1} + n\frac{R_1}{R_2}\frac{kT}{q}\ln(nr).$$ (3)

Also when CMOS technology is applied, at least one bipolar transistor is required to make a bandgap reference [5]. For this application lateral (Fig. 2) or substrate transistors can be used. In the lateral pnp transistor shown in Fig. 2 a gate is used to obtain a thin oxide layer which makes it easy to etch the holes for the emitter and collector diffusions. As compared to the lateral pnp-transistors made in a bipolar process, the CMOS versions do have two main drawbacks:

- There is no buried layer, which gives rise to a relatively large substrate current I_{sub}.

- The $I_C(V_{BE})$ characteristics deviates from the idealised exponential one. This non-ideality has to be expected especially in transistors made in an n-well process, because of the low surface doping. Consequently, high-level effects occur even at rather low current levels.
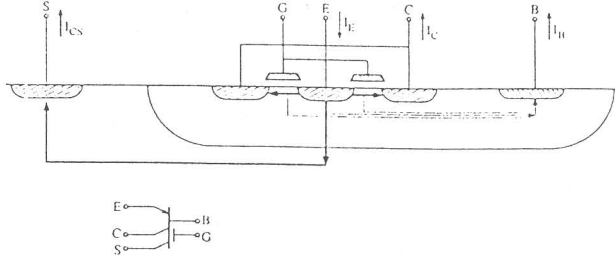
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Fig. 2: A cross section of a lateral pnp-transistor made in an n-well CMOS process

As an example, Fig. 3 shows the $I_C(V_{BE})$ characteristics for a lateral pnp-transistor made in a 1.2μm CMOS process of Alcatel Microelectronics. In a 0.7μm CMOS process the non-ideality of the characteristics are even worse. The (vertical) substrate transistors show a much better performance with respect to the ideality of the $I_C(V_{BE},T)$ characteristics. Therefore, this type of transistor is preferred for generating the V_{BE} and V_{PTAT} voltages in bandgap references. Because all of the collectors of the substrate transistors are connected to the common substrate, special amplifier configurations are required to amplify the PTAT voltage. Fig. 1(b) shows a basic configuration for a CMOS bandgap reference. The generated output amounts to

$$V_{out} \equiv V_{EB2} + \left(1 + \frac{R_2}{R_{PTAT}}\right)(V_{PTAT} + V_{OS}), \qquad (4)$$

where $V_{PTAT} = (kT/q)\ln n = (V_{EB1}-V_{EB2})$ and V_{OS} is the offset voltage of the amplifier A. In the configuration of Fig. 1(b) the current density ratio of Q_1 and Q_2 equals their emitter-area ratio. The main problems of the traditional CMOS bandgap references are caused by the non-idealities of the applied amplifier. In section 3 of this paper it will be shown how these problems can be
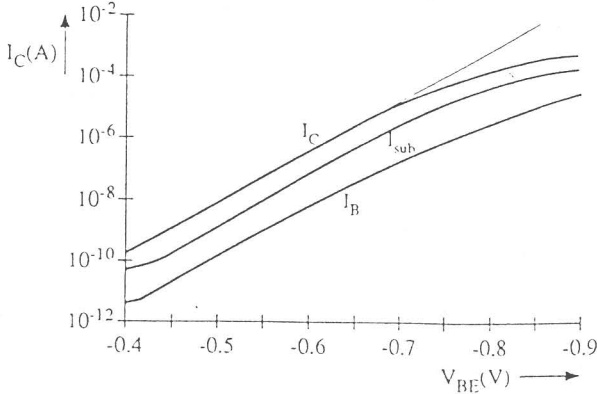

Fig. 3: The $I_C(V_{BE})$ characteristics of a lateral pnp transistor fabricated in an n-well CMOS process (courtesy of Alcatel Microelectronics)

solved, using dynamic techniques. In these dynamic circuits the accuracy is limited by that of the basic signals $V_{BE}(T)$ and $\Delta V_{BE}(T)$.
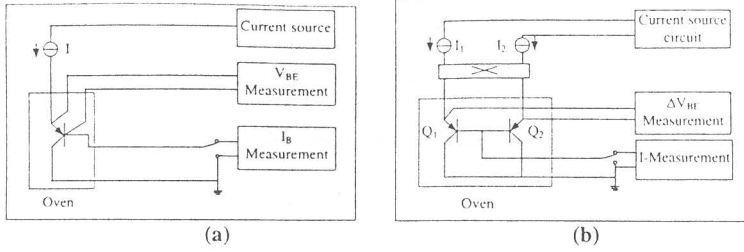
Fig. 4: The test set-ups to measure (a) $V_{BE}(T)$ and (b) $\Delta V_{BE}(T)$

2.2 Characterisation of $V_{BE}(T)$ and $\Delta V_{BE}(T)$

In order to characterise $V_{BE}(T)$ and $\Delta V_{BE}(T)$ for CMOS substrate transistors, we performed a number of measurements for transistors made in a $0.5\,\mu m$ CMOS process of Alcatel Microelectronics. The test set-ups are shown in Fig. 4(a) and 4(b), respectively. In the set-up of Fig 4(b) it holds that $I_2 = 3I_1$. An analogue multiplexer is used to enable cross connection of the two current sources. In this way the effect of a small mismatching between the transistor Q_1 and Q_2 can be eliminated.

As a result Fig. 5 (a) shows the measured ΔV_{BE} voltage normalised with respect to an ideal PTAT voltage versus the current I_1, for various temperatures.
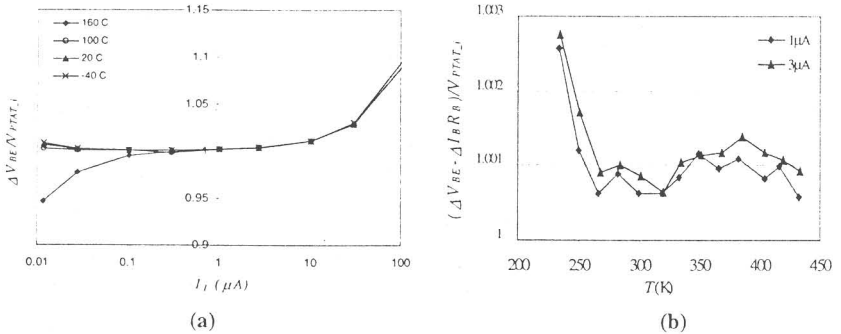

Fig. 5: (a) The measured $\Delta V_{BE}(T)$ voltage normalised with respect to an ideal PTAT voltage versus the biasing current, (b) The same values, but corrected for the base-resistance effect and plotted versus the temperature.

At current levels $I_C > 10\,\mu A$ a large deviation from the ideal value is found. For the main part this is due to the effect of the base resistances, that cause an error $\Delta(I_B R_B)$ which equals

$$\Delta(I_B R_B) = I_{B2} R_{B2} - I_{B1} R_{B1}. \tag{5}$$

It can be shown that the so-called high-level injection only occurs at much higher current levels ($I_{kF} \approx 4$ mA). In fact, using the data plotted in Fig. 5(a) together with the data of $I_B(I_E)$ enables to calculate the value of R_B. Subtracting the values of $\Delta(I_B R_B)$ from the measured values of ΔV_{BE} results in the data plotted in Fig. 5(b), versus the absolute temperature T.

These results allow us to improve the model of $\Delta V_{BE}(T)$ by introducing the so-called emission coefficient n , according to the equation [6]

$$\Delta V_{BE} = \frac{nkT}{q} \ln\left(\frac{J_1}{J_2}\right), \qquad (6)$$

where J_1 and J_2 represent the current densities of Q_1 and Q_2, respectively.

From Fig. 5(b) it can be concluded the $n \approx 1.001$. Furthermore it can be concluded that over the temperature range 250K < T < 430 K, the remaining relative errors in $\Delta V_{BE}(T)$ are less than 400 x 10^{-6}.

Next, the $\Delta V_{BE}(I_C,T)$ characteristics have been evaluated. The measurement results show that the temperature dependency satisfies the well-known equation [2]:

$$V_{BE} = V_{g0}\left(1 - \frac{T}{T_r}\right) + \frac{T}{T_r}V_{BE}(T_r) - \eta\frac{kT}{q}\cdot\ln\left(\frac{T}{T_r}\right)$$
$$+ \frac{kT}{q}\cdot\ln\left(\frac{I_C(T)}{I_C(T_r)}\right), \qquad (7)$$

where $V_{BE}(T_r)$ is the base-emitter voltage at a certain reference temperature T_r, V_{g0} is the extrapolated bandgap voltage at 0 K and η is a constant representing the curvature of the $V_{BE}(T)$ characteristic. From our measurement results, we found the experimental values: $V_{g0} = 1.141$V and $\eta = 4.3$. These values are close to those of npn transistor fabricated in bipolar technology.

From the $V_{BE}(I_C)$ data, the high-level injection parameter I_{KF} and the emission coefficient n can be derived. For our devices under test it has been found that $I_{KF} = 3.7$ mA and $n = 1.001$. The latter value is equal to that found from the ΔV_{BE} measurements.

2.3. Long-term stability of $V_{BE}(T)$ and ΔV_{BE}

Mechanical stress is the main cause of the long-term drift and hysteresis during thermal cycling of bandgap references [2]. Recently, it has been found by Fruett [7] that the PTAT voltage is much less sensitive to stress than the base-emitter voltage itself. Therefore, to get a better performance with respect to these important properties, measures have to be taken to reduce the mechanical stress or to optimise the transistor design for the lowest piezo-junction effect.

3. Dynamic voltage references

In many applications the voltage references are part of a measurement system to determine an unknown voltage V_x. Especially in this case, the problems of CMOS amplifiers can be solved by using dynamic methods to measure the basic signals V_{BE}, ΔV_{BE} and the offset voltage V_{OS}.

In [4] and [8] a basic set-up for such a system is presented, according to the principle of Figure 6. The voltages V_X, V_{BE}, V_{PTAT} and V_{OS} are converted to the time domain by a linear voltage-to-period converter. When the output periods during the successive measurements are t_X, t_{BE}, t_{PTAT} and t_{OS}, respectively, then the final measurement result F amounts to

$$F = \frac{t_x - t_{os}}{t_{BE} + At_{PTAT} - (A+1)t_{os}} = \frac{V_x}{V_{ref}} \qquad (8)$$

The micro-controller is used to store the various measurement data in its memory and to perform the algorithmic processing. Dynamic techniques are applied to amplify the small voltages [10], to divide the large voltage [9] and to generate an accurate PTAT voltage, as shown in [8]. Application

of these dynamic techniques solves the problems of the mismatching, offset and drift of the CMOS amplifier components. By applying chopping, at a sufficiently high frequency, after filtering and demodulation also the effects of 1/f noise and low-frequency interference are eliminated.
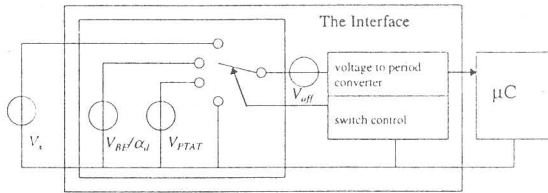

Figure 6: A basic set-up for a dynamic voltage measurement system

Presently, a CMOS circuit for voltage processing is designed. The embedded voltage reference and on-chip temperature transducer are calibrated, using programmable switches, which modify the emitter are of one of the substrate transistors in the V_{BE} generator.

4. Discussion and Conclusions

The paper show how accurate bandgap references and temperature sensors can be realised, using low-cost CMOS technology. The substrate pnp transistors are very suited to generate the basic signals V_{BE} and ΔV_{BE} of such a reference in an accurate way. The biasing currents of these transistors have to be chosen within a limited dynamic range to limit the base-resistance and low-level effects. The problems of CMOS technology, such as mismatching of components and 1/f noise, can be eliminated by applying continuous auto-calibration, dynamic element matching and chopping.The described techniques have been especially developed for measurement systems, where it is not necessary to generate a real time voltage output. The accuracy of these CMOS references can be as good or even better as that of the bipolar ones.

5. References

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