Addressing System of the Look-Up-Table for Digital Waveform Synthesis

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1. Abstract

The purpose of this article is to describe a particular aspect of the design of an arbitrary waveform generator based on the method of digital synthesis. Similar generator was built at the Department of Electronic Engineering and Technology of the Technical University of Sofia. It covers the frequency range of 5mHz up to 1MHz. The samples of the signal that must be synthesised are contained in a memory that is called look-up-table (LUT). The main problem discussed here is the construction of the addressing system to this memory. Two methods for realising it are shown and how each of them affects the features and output characteristics of the generator is explained.

2. Introduction

Arbitrary waveform generators are needed in several applications. But most available waveform generators are designed for special-purpose applications and they can deliver a limited class of signals. The easiest way to realise a truly general-purpose waveform generator is to synthesise the waveforms digitally and to use a microcomputer to control each function of the instrument.

The digital synthesis of a signal is the opposite process of signal digitalisation. The basic idea consists of the following. The values of a given signal are calculated for equal time intervals. These values are called samples and are stored in adjacent locations of a high-speed memory that is called look-up-table (LUT). The content of this memory is cyclically addressed in order to drive a D/A-converter, which generates the output waveform (Fig. 1).

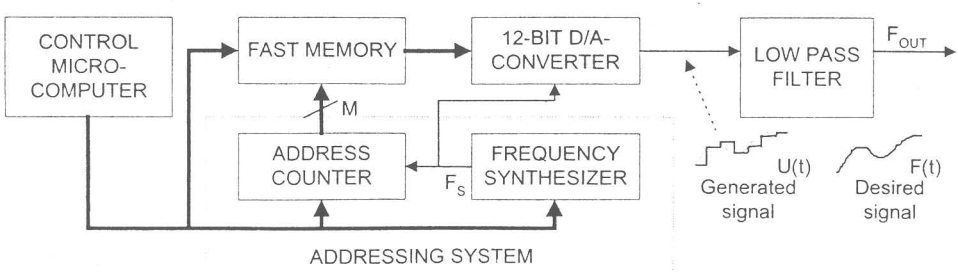

Figure 1. General block diagram of an arbitrary waveform generator.

The output of the converter is a staircase-like approximation of the desired signal because the output of the D/A-converter remains fixed between two consecutive clock edges. The frequency at which the look-up-table is updated is the same as the clock frequency of the D/A-converter. It is called sample frequency.

The two main error sources causing the differences between the output signal U(t) and the desired signal F(t) are quantization and sampling. The amount of quantization error depends on the resolution of the D/A-converter. Its influence is measured by the signal-to-noise ratio (SNR) due to quantization and may be calculated by the following equation:

$$\mathrm{SNR\ (dB)} = 6.02n + 1.76 \qquad (1),$$

where **n** is the resolution of the converter.

The contribution of sampling to the output noise depends on the clock frequency of the converter. Because the DAC doesn't change its output between two consecutive clock edges, it actually realises signal sampling with a zero-order holding. If such a system is used for approximation of any band-limited signal, it is proved that the output spectrum comprises harmonics which amplitude is expressed by the following equation:

$$a_K = 2\frac{\sin\frac{k\pi}{N}}{k\pi}\sum_{l=0}^{N-1}\cos\frac{2\pi l}{N}\cos\left(\frac{k\pi}{N}(2l+1)\right) \qquad (2).$$

Here, K is the order of a harmonic and N is the ratio between the period of the output signal and the sampling period – $N = T_{OUT} / T_S$. Consequently the output spectrum doesn't depend on the frequency of the synthesised signal or on the clock frequency of the system, but only on the number of samples per period of the signal. Calculations based on the above equation confirm that the only non-zero harmonics are those of order $\mathbf{m(N}f_S) \pm f_{OUT}$, where **m** is a whole number. Their amplitude decreases whith the increasing of N. This is represented at figure 2.

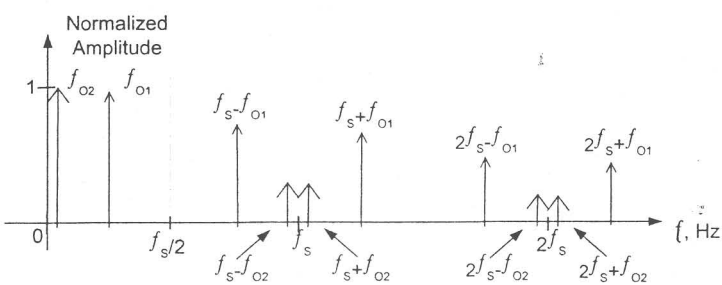

Figure 2. Theoretical spectrum of a sampling with zero-order holding system.

3. Choosing an addressing system

- **Direct approach.**

Waveform generators based on digital synthesis are divided in two groups according to the addressing system of the LUT. These are arbitrary generators and DDS-generators.

The addressing system of the arbitrary generators is based on an address counter and a frequency synthesizer as shown at figure 1. All the memory locations are addressed sequentially. Hence the frequency of the output signal is determined by the length of the address counter and the programmable sample frequency:

$$F_{OUT} = F_S/2^M \qquad (3).$$

In this equation M is a constant for a given system and the output frequency is proportional to the frequency of the programmable synthesizer only. Equation 3 shows that for M=12 and F_S equal to 50MHz, the output frequency is 12.2kHz. We use this type of the addressing system for synthesizing single-cycle signals with large duration if we have a programmable sample clock source. But if we need shorter output period, we must change the contents of the LUT, writing in it less samples per period. We must read the LUT at the maximum sample frequency and also restrict the output value of the address counter by means of an address comparator in order to read only the meaningful samples. Thus the addressing system becomes more complex.

We found it convenient to use FIFO-type of memory which integrates both the address counter and the LUT itself (figure 3).

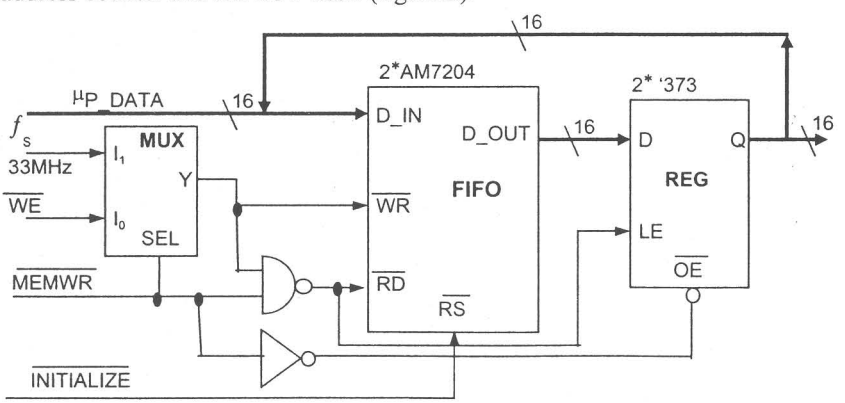

Figure 3. Addressing system utilizing FIFO memory.

This memory maintains two automatic address pointers for the current locations of read and write accesses. These pointers are initialized to zero every time they reach the last address. The flags for overflow and empty stack are set depending entirely on the difference between the read and write address pointer. If the microprocessor writes ***K***-count samples then this difference will equal ***K***. When

synthesizing the desired signal, the memory is read at the rising edge of the sample clock (f_S) and the output data is written into the next empty locations at the falling edge of the same clock. In this way the difference between the two pointers is constant and equals K. Therefore K is the number of samples per period of the output signal.

While this architecture is fairly simple, it needs a programmable sample clock. The need of reloading the LUT with another samples for generating different frequency of the same waveform makes it impossible to realize frequency sweep of a given signal.

- **Direct digital synthesis.**

The second approach of building the addressing system is known as the method of direct digital synthesis (DDS). It is based on the idea of non-sequential addressing of the LUT. The memory comprises the maximum number of samples that will be used for synthesizing one period of the signal at the lowest output frequency. The look-up-table is addressed at a constant speed. According to the desired output frequency we skip certain amount of locations of that table. As we skip more locations we have less samples per period. Consequently at a constant sampling frequency, the output frequency is proportional to the number of the omitted addresses. Figure 4 represents the architecture of the generator we build.

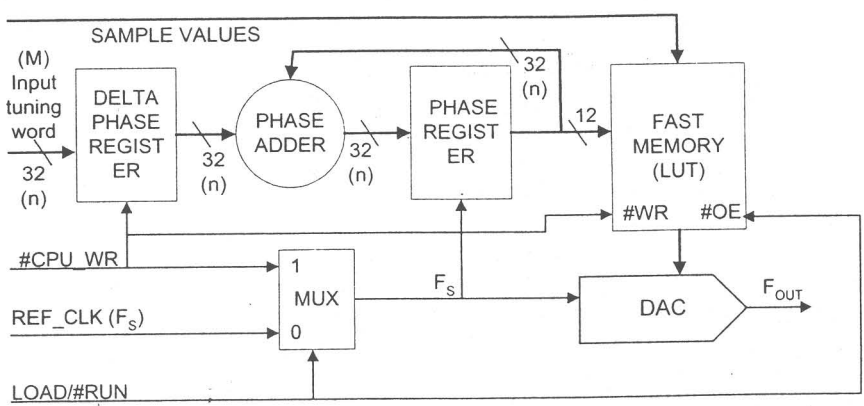

Figure 4. DDS based waveform generator.

In the block diagram above the phase adder and the phase register form a phase accumulator. Its output provides the address location (in the look-up-table) for the current sample – it actually corresponds to the current phase of the output signal. The tuning word is latched in the delta phase register and is added to the current value of the phase register at every rising edge of the sample clock. The tuning word equals the number of samples that must be skipped and represents the speed of advancing

the current phase between two successive rising edges of the sample clock. The output frequency is calculated by the following equation:

$$F_{OUT} = M\frac{F_S}{2^N} \qquad (3).$$

Here M is the integer value of the tuning word and N is the resolution of the phase accumulator. While N is a constant we can modify the output frequency with great precision simply by changing the tuning word M. For example in our case we derive the sample clock from a fixed frequency crystal oscillator at 16MHz. We utilise 32-bit phase accumulator consequently N is 32. Under these conditions the least possible frequency is generated at M equal to 1 and is approximately 4mHz. This is also the frequency resolution of the synthesiser for the entire range. If we tune the M to 268435254, we will get 1MHz at the output, having 16 samples per period.

The system shown at figure 4 operates as follows - the fast memory is loaded with the samples of the desired waveform under control of a CPU. While this is in progress, the LOAD/#RUN signal is set to one. The tuning word equals one and the phase accumulator issues successive memory addresses at every rising edge of the CPU clock. After the look-up-table is loaded the CPU adjusts the frequency by writing a proper tuning word. When signal generation starts, the LOAD/#RUN signal is cleared to zero and the phase accumulator is clocked with the sample frequency. The outputs of the fast memory are enabled in this mode only and write accesses to that memory are prohibited.

The architecture shown at figure 4 is implemented on a programmable logic – Xilix-XC4003 FPGA device. It is because the conventional logic devices are not suitable to realize 32-bit accumulator operating at 20MHz. We also incorporate some additional control logic into the same chip. It is relevant to the interface of the supervising microcontroller and the user.

4. Conclusion

For final realization of our arbitrary waveform generator we chose the second method of building the addressing system. We consider that DDS is more suitable for the case because of several reasons. Simple, yet precision reference clock generator - temperature compensated crystal oscillator at 16MHz. Achieving a wide frequency range – 4mHz – 1MHz. High frequency resolution – equal to 4mHz through the whole frequency range. Ease of programming the output frequency and waveform. Inherent to the DDS are frequency sweep, frequency and phase modulation. Thus, a DDS system based on a programmable logic (FPGA) allows functionality upgrade.

5. Reference

- A.Oppenheim, R.Schafer, *Digital Signal Processing*, Prentice-Hall, New Jersey,1975.
- ANALOG DEVICES, "High Speed DACs and DDS", *System Application Guide*, Pr.Hall, N.J., 1993.
- AMD, *CMOS FIFO Memory Products Databook*, 1992.
- D.Caviglia, G.Donzellini, "Design and Construction of an Arbitrary Waveform Generator", *IEEE Trans. Instrumentation and Measurement*, vol. IM-32, No. 3, pp. 398-403, September 1983.