A Novel Switched – Capacitor Front End for Capacitive Sensors with Wide Dynamic Range

Gerard C.M. Meijer, Ventzeslav P. Iordanov
Delft University of Technology, Faculty of Information Technology and Systems, Electronics Research Laboratory, Mekelweg 4, 2628 CD Delft, The Netherlands

Abstract
This paper describes a new switched–capacitor (SC) front end for capacitive sensors based on a 1st order relaxation oscillator (modified Martin oscillator). In conventional front ends the input integrator limits the dynamic range of the front end. In this paper two novel designs of front ends with much wider dynamic range are presented. Experimental results show a non–linearity of less then $200x10^{-6}$ over the range of 0 – 1nF.

Introduction

A sensor with integrated electronics and an off-chip microprocessor (microcontroller) used to communicate with the user and modify its response is called "smart" sensor. A variety of interface circuitry has been developed for such "smart" sensors. In the specific case of capacitive sensors it seems that switched–capacitor circuits are the best option for building interface electronics because their fabrication process is compatible with the sensors [1-6]. All these interfaces consist of capacitors– controlled modulators and digital control circuits. For the modulators in smart signal processing (SSP), for capacitive measurement, it is common to use 1st order relaxation oscillators. Especially the modified Martin oscillator and charge–balance oscillators are preferable. The output signal of the integrator should be well within the supply voltage range. Because of distortion at this signal the linearity of the *CPC* (charge-to-period converter) will be suppressed. This limitation of the integrator limits automatically the dynamic range of the transducer [7].

A Novel Concept

In this papers a new type oscillator is proposed, which offers a solution for the problem stated above. The following consideration forms the basic idea for the circuit:
The problems are caused by the fact that charge of the measured capacitor C_x is dumped in a very short time into C_{int}. If this process could be spread out over the available time, then the amplitude of the output voltage will be

lower. If the output voltage of the integrator is "watched" actively and if this output voltage controls the charge current then it is possible to avoid clipping. With the control circuit mentioned above, the output signal of the integrator gets a weird shape, but this is of no importance as long as the *CPC* stays in its linear region in such a way that the period (or the frequency) depends linearly on the capacitance to be measured. Fig. 1 shows a simple solution for the problem.

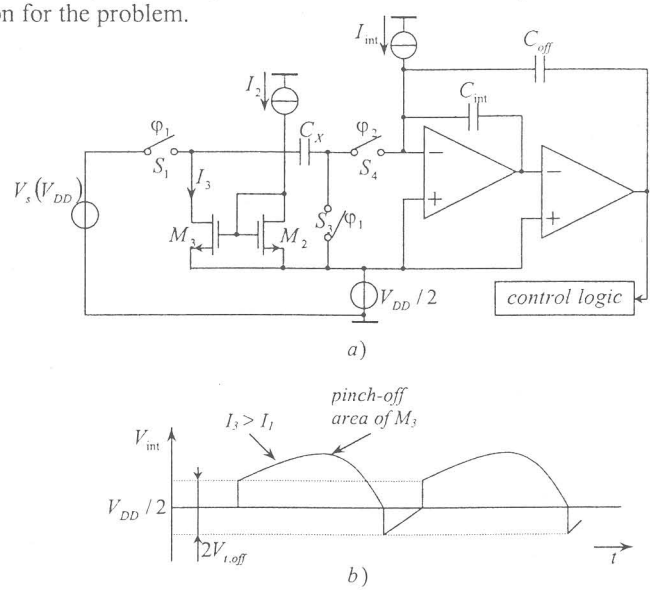

Figure 1: A new concept for increasing the dynamic range a) and the output of the integrator b).

The circuit works as follows:
The voltage V_s charges the measured capacitor C_X, when the switches S_1 and S_3 are closed. Next, these switches are opened and S_4 is closed. Now the charge from C_X is transferred to integrator capacitor C_{int} by the help of a current I_2. During the same time the I_{int} discharges C_{int}. Actually the current, which flows through C_{int} is given by $I_{dif} = I_3 - I_{int} \approx I_2 - I_{int}$ (if the current mirror works in the active region). I_2 is chosen a little bigger then I_{int}, because if the ratio I_{int}/I_2 is bigger than *1* then the output of the integrator will reach the comparator level before all charge from measured capacitor is transferred to C_{int}. Because of this charge transfer the voltage on the drain of

M_3 decreases. Below the pinch-off area, the current I_3 decreases and when $I_3 < I_{int}$ holds the output voltages of the integrator V_{int} decreases.
As soon as the comparator level is reached S_4 is opened, S_1 and S_3 are closed, and the sampling of V_s starts all over again.

Improved circuit Configuration

The purpose of the current mirror is to get $I_{dif} << I_{int}$, so the voltage sweep over C_{int} is limited. This goal is better achievable if I_2 is dependent on V_{int}. This can be achieved if an inverting voltage-to-current converter is added to the circuit (Fig. 2).

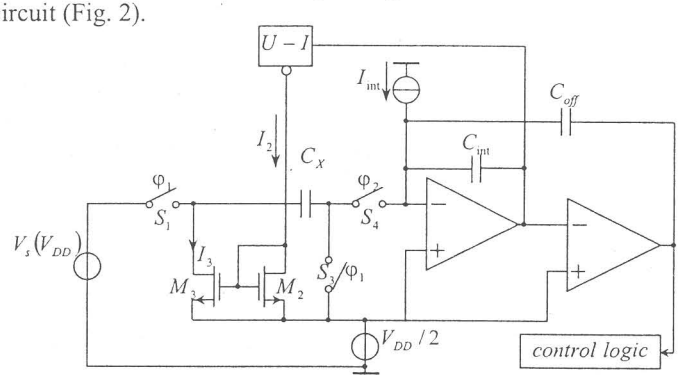

Figure 2: The circuit with I_2 controlled by the output of the integrator.

The requirement to the U-I converter is not very critical and it is allowed to be non- linear. A simple OTA can be used (Fig. 3).

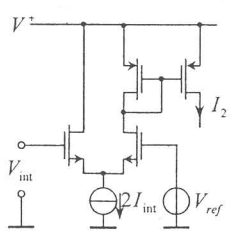

Figure 3: Inverting Voltage-to-Current Converter.

If V_{int} is low, than $I_2 \approx 2I_{int}$ and V_{int} increases linearly. The saturation occurs if $V_{int} \approx V_{ref}$ ($I_2 \approx I_{int}$ – Fig. 4).

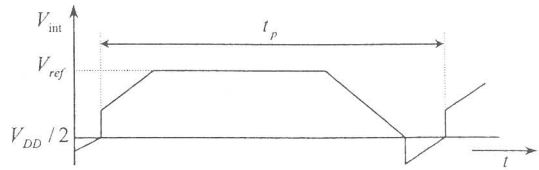

Figure 4: The output signal of the integrator.

Although the output voltage of the integrator has a strange shape, the Operational Amplifier operates in linear region. The period of the oscillator depends linearly on the capacitance to be measured. The charge balance principle is still valid, so during the period t_p the charge through current source I_{int} equals $I_{int}*t_p$. This charge has to be the same as the charge that is transported through C_X and which is equal to $V_{DD}*C_X$, so

$$t_p = \frac{V_{DD}C_X}{2I_{\text{int}}} + 2\frac{V_{DD}C_{off}}{I_{\text{int}}} = \frac{V_{DD}(C_X + 4C_{off})}{2I_{\text{int}}} \qquad (1)$$

Applying the three-signal technique can easily skip the part, which is proportional to the offset (as it shown below).

Measurement setup

The measurements of resolution and non-linearity have been performed with the measurement setup as shown in Fig. 5. The system is based on external multiplexer, sensing and reference element, the front-end, a counter and a PC.

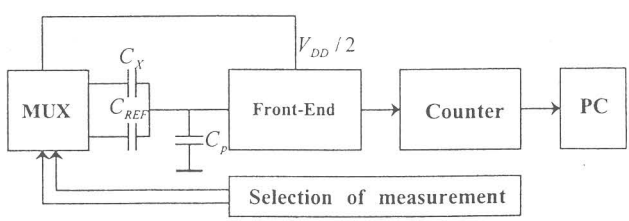

Figure 5: Measurement setup.

Non-linearity and resolution

The calculation of the non-linearity is based on four measurements. In addition to the measurement of the offset signal E_{off}, the signals $E_{X1}+ E_{off}$

and $E_{X2}+ E_{off}$ are measured separately, and, finally, the sum $E_{X1}+ E_{X2}+ E_{off}$ is measured. This results in four measurement phases:

1. Measurement of $T_{off} = GE_{off}$
2. Measurement of $T_{X1} = G(E_{off} + E_{X1})$
3. Measurement of $T_{X2} = G(E_{off} + E_{X2})$
4. Measurement of $T_{X1+X2} = G(E_{off} + E_{X1} + E_{X2})$

The non-linearity λ is now defined by:

$$\lambda = \frac{T_{X1} + T_{X2} - 2T_{off}}{T_{X1+X2} - T_{off}} - 1 \qquad (2)$$

The non-linearity in the range 0 – 1000pF has been measured with randomly chosen pairs of equal capacitors.

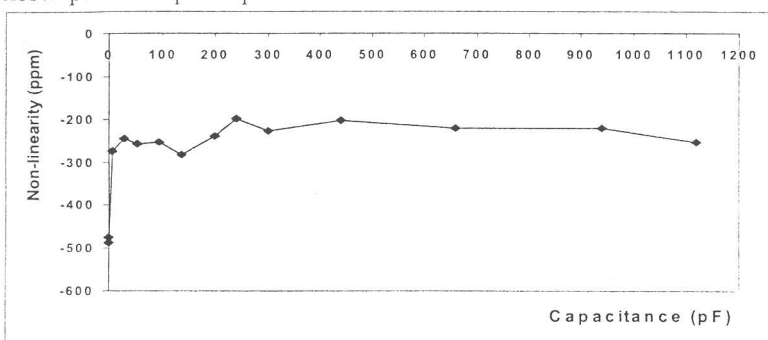

Figure 6: The non-linearity versus the different pairs of capacitors.

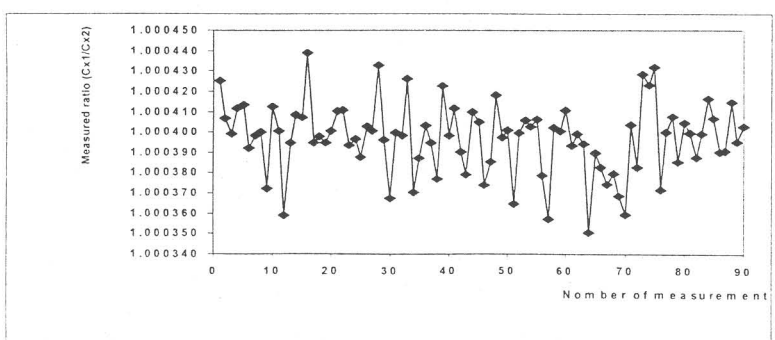

Figure 7: Resolution after the calculations related to the three-signal technique for ninety different measurements.

The resolution (Fig. 6) is calculated, in a way related to the three- signal technique, for a pair of capacitors, 560pF each. As it shown in Fig. 7 the resolution amounts to 16 bits.

Conclusions

In this papers two novel designs of switched–capacitor (SC) front-ends for capacitive sensors with extended dynamic range are presented. The circuits are based on a 1st order relaxation oscillator (modified Martin oscillator). In conventional front-ends the input integrator limits the dynamic range of the front-end. The problems are caused by the fact that the charge of the measured capacitor is dumped in a very short time into the integrator capacitor. As a consequence, the output of the integrator is saturated and the linearity of the *CPC* (capacitance-to-period converter) is suppressed. In our solution the output voltage of the integrator is "watched" actively and depending on the value of the output voltage, the charge current, which transfers the charge of the measured capacitor to the integrator capacitor, is controlled. So, the charge-transfer process is spread out over the available time. With the control circuit mentioned above, the output signal of the integrator gets a weird shape. Nevertheless, the *CPC* stays in its linear region for a wider range of measured capacitance. Experimental results show a non-linearity of less than 300×10^{-6} over the range of 0 – 1nF and resolution of 16 bits.

References

[1] K. Martin, "**A Voltage – Controlled Switched – Capacitor Relaxation Oscillator**", *IEEE J. of Solid State Circuits*, vol. SC-16, pp. 412-414, August 1981.

[2] Kazuyuki Kondoh and Kenzo Watanabe, "**A Switched – Capacitor Interface for Capacitive Sensors with Wide Dynamic Range**", *IEEE Trans. Instr. and Meas.*, vol. 38, No. 3, pp. 736-739, June 1989.

[3] J. van Drecht and G.C.M. Meijer, "**Relaxation Oscillator**", patent appl., Fundamental Research on Matter (FOM), (91.01076), June 21, 1991.

[4] F.N. Toth and G.C.M. Meijer, "**A low-cost smart capacitive position sensor**", *IEEE Trans. Instr. and Meas.*, vol. IM-41, pp.1041-1044, December 1992.

[5] H. Matsumoto, H. Shimizu and K. Watanabe, "**A Switched – Capacitor Charge - Balancing Analog – to – Digital Converters and Its Application to Capacitance Measurement**", *IEEE Trans. Instr. and Meas.*, vol. IM-36, pp. 873-878, December 1989.

[6] A. Cichocki and R. Unbehauen, "**A Switched – Capacitor Interface for Capacitive Sensors Based on Relaxation Oscillators**", *IEEE Trans. Instr. and Meas.*, vol. 39, No. 5, pp. 797-799, October 1990.

[7] Frank M.L. van der Goes, "**Low-cost smart sensor interfacing**", Ph.D. Thesis, Delft University of Technology, Apr. 1996.