

# A Method for Minimizing Capacitor Mismatch Error In a Charge Redistribution DAC.<sup>1</sup>

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## Abstract

A simple yet efficient method for improving the linearity of a two - capacitor charge redistribution digital - to - analog converter (DAC) is presented. This method implements consecutive swapping of the capacitors (in terms of order of operation) for each bit being converted. The simple technique of interchanging the voltages on the capacitors proves useful for minimizing mismatch error. Although this error is not entirely compensated, the linearity of the DAC is improved considerably.

A major advantage of the method is its simplicity and effectiveness for high - resolution applications.

Simulations have been performed and have proved the feasibility of this new technique.

*Introduction.* One of the most economical (in terms of area, digital – to – analog converters is the two-capacitor charge redistribution DAC [1]. It is suitable for low-resolution low - speed applications and is easily implemented in standard CMOS technology. Besides, this DAC has the advantage of easy matching compared to weighted binary arrays. Here, capacitor mismatch is a major source of error. This hurdles the realization of high-resolution applications.

Many techniques have been described for compensating the capacitor mismatch. Some implement a calibration cycle and storing digital correction terms in RAM [2]. Another method to improve linearity is to optimize the switching sequence for each input vector [3]. Since some kind of estimation is required, time and area are wasted for the completion of these correction cycles. Many other solutions [4] such as the splitting algorithm are described [5]. It eliminates capacitor mismatch. However, this requires a ROM or an algorithmic unit to control the switching sequence, which belittles the DAC's main advantage – its small size.

The proposed method does not remove capacitor mismatch error, but it does improve linearity a lot. What is important – it does not withal implement much additional elements and is as simple as the conversion algorithm itself.

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## I. Two – capacitor charge redistribution DAC basics.

The basic schematic of a charge redistribution DAC is shown in fig.1. It consists only of two equal - valued capacitors and a few switches. The conversion is carried out as follows:

In the beginning the reset switch is closed. The digital code being converted is applied with its least significant bit first. The value of this bit drives switches bit '1' and bit '0'. Next  $\Phi 1$  is activated and capacitor C1 acquires  $V_{ref}$  or ground. During phase two  $\Phi 2$  is closed and the charge stored on C1 is distributed among C1 and C2. If  $C1 = C2$  exact division by two is accomplished. It can thus be shown that after N cycles the total output charge over C2 will be:

$$Q_{c2} = C_2 V_{ref} \sum_{n=1}^N b_n 2^{n-N-1}$$

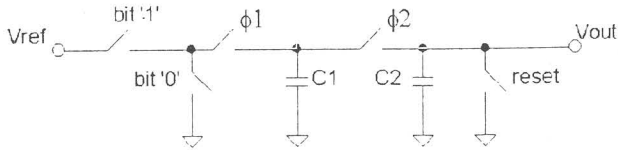


Fig.1

This equation gives the output of digital – to – analog converter. The problem here is that C1 and C2 must have equal values. Unfortunately the aforementioned condition cannot be guaranteed. This leads to conversion error. Minimizing this error requires additional digital circuitry and hence - additional area. A solution must be found that keeps the DAC's main advantage – its small size. The authors of this paper propose a method for reducing the influence of the capacitor mismatch error on accuracy without sacrificing chip area.

## II. Voltage interchanging

This method does not remove capacitor mismatch error but it does reduce it significantly. It consists of two consecutive cycles, each of which produces a voltage according to the selected charge pattern (i.e. which capacitor is chosen to be the charging one). Next, these two voltages are interchanged and applied to  $C_1$  and  $C_2$ . The whole algorithm is described below.

Consider the following schematic diagram

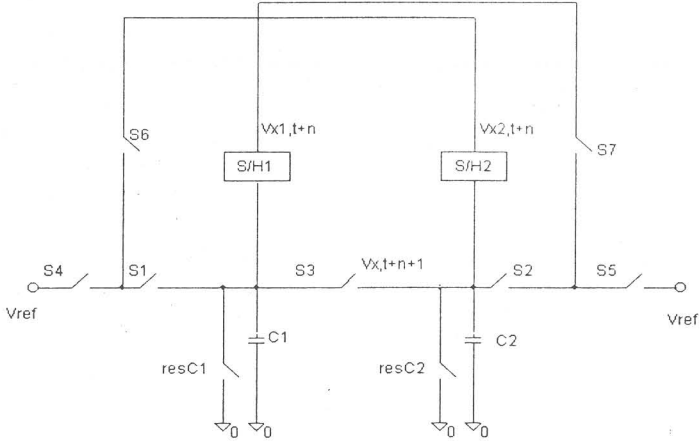


Fig. 2

In the beginning of the conversion  $Q_{C1}^t=0$  and  $Q_{C2}^t=0$ . Let the least significant bit is  $b_n$ . Switch S4 is closed if  $b_n$  is '1' and switch resC1 is closed if this bit equals '0'. This charges  $C_1$  with

$$Q_{C1}^{t+1} = C_1 V_{ref} b_n$$

$Q_{C2}^{t+1}$  remains 0. After switch S3 is closed the stored charges are summed, which results in

$$Q^{t+1} = C_1 V_{ref} b_n + 0 = V_{x1}^{t+1} (C_1 + C_2)$$

$$V_{x1}^{t+1} = V_{ref} b_n \frac{C_1}{C_1 + C_2} \quad \text{This voltage is stored in S/H1. The operation is}$$

repeated but this time by charging  $C_2$  to  $V_{ref}$  (or ground). By analogy, for  $V_{x2}^{t+1}$  we obtain

$$V_{x2}^{t+1} = V_{ref} b_n \frac{C_2}{C_1 + C_2} \quad \text{This voltage is stored in S/H2. Next, switches S6/S1}$$

and S7/S2 are closed to enable  $C_1$  to charge to  $V_{x2}^{t+1}$  and  $C_2$  to charge to  $V_{x1}^{t+1}$ . This results in

$Q_{C1}^{t+2} = C_1 V_{x2}^{t+1}$  and  $Q_{C2}^{t+2} = C_2 V_{x1}^{t+1}$ . After the closure of S3 the total charge will be

$$Q^{t+2} = C_1 V_{x2}^{t+1} + C_2 V_{x1}^{t+1} = V_x^{t+2} (C_1 + C_2)$$

$$V_x^{t+2} = \frac{C_1 V_{x2}^{t+1} + C_2 V_{x1}^{t+1}}{C_1 + C_2} = \frac{C_1 V_{ref} b_n \frac{C_2}{C_1 + C_2} + C_2 V_{ref} b_n \frac{C_1}{C_1 + C_2}}{C_1 + C_2} = V_{ref} b_n \frac{2C_1 C_2}{(C_1 + C_2)^2}$$

$V_x^{t+2}$  is stored in both sample-holds. Next, bit  $b_{n-1}$  determines the position of

S4 and resC1, thus charging  $C_1$  to  $V_{ref}$  or discharging it to ground.  $C_2$  still has its voltage equal to  $V_x^{t+2}$ . The charges on both capacitors is as follows

$Q_{C1}^{t+3} = C_1 V_{ref} b_{n-1}$  and  $Q_{C2}^{t+3} = C_2 V_x^{t+2}$ . After the closure of S3 the total charge will be  $Q^{t+3} = C_1 V_{ref} b_{n-1} + C_2 V_x^{t+2} = V_{x1}^{t+2} (C_1 + C_2)$

$$V_{x1}^{t+2} = \frac{C_1 V_{ref} b_{n-1} + C_2 V_x^{t+2}}{C_1 + C_2} \text{ This voltage is stored in S/H1. Now switches S6}$$

and S1 are activated and  $C_1$  is charged to  $C_1 V_x^{t+2}$  (S/H2 still holds  $V_x^{t+2}$ ). Switches S5 (or resC2) and S2 are also closed to give  $C_2$  the charge of  $C_2 V_{ref} b_{n-1}$ . Then, after redistribution,  $V_{x2}^{t+2}$  is equal to

$$V_{x2}^{t+2} = \frac{C_2 V_{ref} b_{n-1} + C_1 V_x^{t+2}}{C_1 + C_2} \text{ This voltage is stored in S/H2. Then switches}$$

S6/S1 and S7/S2 are closed again. This produces the following charge on the capacitors

$Q_{C1}^{t+3} = C_1 V_{x2}^{t+2}$  and  $Q_{C2}^{t+3} = C_2 V_{x1}^{t+2}$ . After the closure of S3 the total charge will be

$$Q^{t+3} = C_1 V_{x2}^{t+2} + C_2 V_{x1}^{t+2} = V_x^{t+3} (C_1 + C_2)$$

$$\begin{aligned} V_x^{t+3} &= \frac{C_1 V_{x2}^{t+2} + C_2 V_{x1}^{t+2}}{C_1 + C_2} = \frac{C_1 \frac{C_2 V_{ref} b_{n-1} + C_1 V_x^{t+2}}{C_1 + C_2} + C_2 \frac{C_1 V_{ref} b_{n-1} + C_2 V_x^{t+2}}{C_1 + C_2}}{C_1 + C_2} = \\ &= \frac{2C_1 C_2 (V_{ref} b_{n-1} + V_x^{t+2})}{(C_1 + C_2)^2} = V_{ref} b_{n-1} \frac{2C_1 C_2}{C_1 + C_2} + V_{ref} b_n \frac{(2C_1 C_2)^2}{(C_1 + C_2)^4}. \end{aligned}$$

If we designate  $\frac{2C_1 C_2}{(C_1 + C_2)^2}$  as  $w$  then the following equation results

$$V_x^{t+k+1} = V_{ref} \sum_{k=0}^N b_{n-k} w^{k+1}$$

Let us compare the accuracy achieved by this method to the one without correction. Consider  $C_1$  and  $C_2$  to have maximum deviations of  $\Delta C$  from their nominal value. In the conventional method the coefficient that is required to have a value of  $1/2$  is  $\frac{C_1}{C_1 + C_2}$ .

If we represent  $C_1$  and  $C_2$  by means of a value  $C$  and an error capacitance of  $\Delta C$  then we will obtain

$\frac{C \pm \Delta C}{C \pm \Delta C + C \mp \Delta C} = \frac{C \pm \Delta C}{2C} = \frac{1}{2} \pm \frac{\Delta C}{2C}$ . The error is introduced by the second term.

When swapping is applied these equations will look like

$$\frac{2(C \pm \Delta C)(C \mp \Delta C)}{4C^2} = \frac{C^2 \mp C\Delta C \pm C\Delta C - \Delta C^2}{2C^2} = \frac{1}{2} - \frac{\Delta C^2}{2C^2}.$$

It is evident that an accuracy gain of  $C/\Delta C$  is achieved.

For the sake of accuracy  $\Delta C/C < 1\text{LSB}$ , i.e.  $\Delta C/C < 1/2^N$  (where  $N$  is the resolution of the DAC) in the conventional method. If we implement the algorithm described above this restriction is not so stringent.

$$\frac{\Delta C^2}{C^2} < \frac{1}{2^N} \Leftrightarrow \frac{\Delta C}{C} < \sqrt{\frac{1}{2^N}}$$

### III. Results.

The following diagram shows the number of achievable bits by the DAC versus capacitor mismatch.

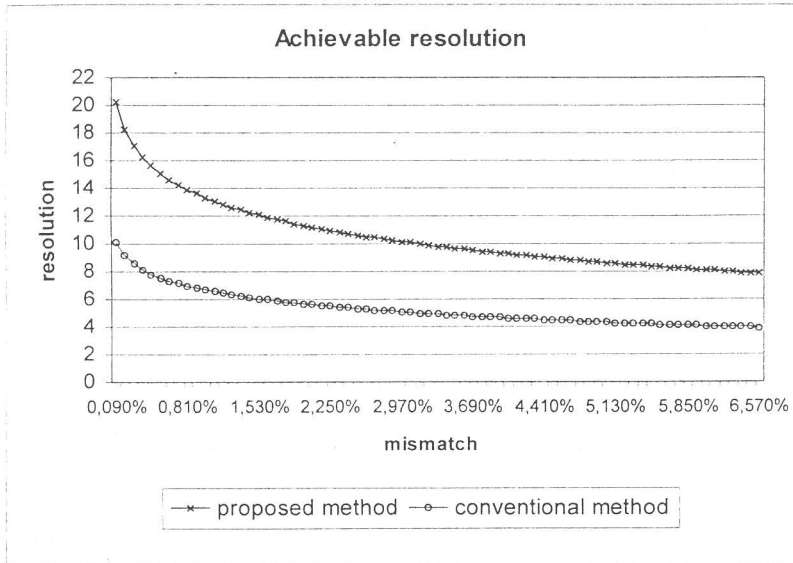


Fig.3

Simulations have been performed to prove the feasibility of the proposed technique. Mismatch of 10% was chosen. We tested the worst case where both capacitors had the error capacitance summed with and subtracted from (for  $C_1$  and  $C_2$  respectively) the ideal capacitance  $C$ . The diagram shows the division by two of  $V_r=3\text{V}$ . The erroneous voltages (seen at  $1,5\mu\text{s}$  and  $2,5\mu\text{s}$ ) are placed almost symmetrically around the averaged one. The calculated output voltage is  $1,485\text{V}$ .  $V_{x1}$  and  $V_{x2}$  are equal to  $1,65\text{V}$  and  $1,35\text{V}$  respectively. The selection of a large  $\Delta C/C$  was made on purpose aiming more illustrative results.

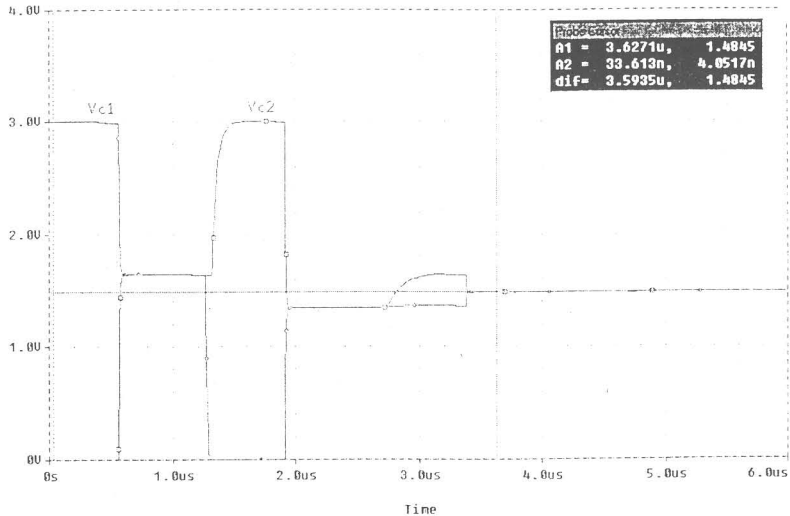


Fig.4

#### IV. Conclusion.

A simple and efficient method for reducing the influence of the capacitor mismatch error in a charge redistribution DAC has been described. Its main advantage is that it does not improve linearity at the expense of chip area, but rather at the expense of the slightly increased algorithmic complexity.

The obtained results show that this method is useful for designing digital – to analog converters of higher than 8 bits of resolution.

Due to the short correction, cycle the speed of operation could be (almost) as high as in the conventional method.

The described correction technique does not require precise design and hence the DAC could be easily implemented in a standard low – cost CMOS process.

## References

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