A CMOS Schmitt Trigger with Current Controllable Voltage Threshold and Dynamic Hysteresis

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Abstract - A novel CMOS Schmitt Trigger with Input Stage architecture appropriate for current control of the threshold voltage is proposed and its feasibility on CMOS technology is studied. The two main advantages of the new circuit (a good opportunity for current control of the input threshold and a very good dynamic noise immunity) are demonstrated.

I. INTRODUCTION

The CMOS Schmitt triggers such as in Fig.1 [1] are widely used in complex analog and analog-to-digital electronic circuits. An improved variant of this circuit, which ensure a "dynamic hysteresis", is proposed and investigated in [2](Fig.2) by the first author. Using this CMOS Schmitt trigger the new type of parallel analog-to-digital converter is proposed in [3].

One drawback of these circuits is that their threshold can be controlled only by changing the W/L ratio of the MOS transistors Mn and Mp, representing the input inverter.

To overcome this problem in the present paper is proposed, analyzed, and studied a CMOS Schmitt Trigger with Current Controllable Voltage Threshold and Dynamic Hysteresis.

II. THE NEW CIRCUIT

The proposed circuit is shown in Fig.3. It combines an input inverter stage and two feedback loops. The current Iref controls the load of the input transistor Mn. By this way it determines the transfer characteristic switching points (Fig.4), which are the voltage threshold of the trigger. Both feedbacks

interact through transistors M1 and M2. The positive feedback PF allows reaching maximal switching rate. When the raising input signal reaches the input inverter (Mn and Mp) threshold (Fig.5), the PF switches the transistor M1 from off to on and thanks to the inherent hysteresis the input is blocked just after the start of the switching process. Hence it is not susceptible to input noises. The hysteresis lasts till the arrival of the delayed negative feedback NF signal. It switches from on to off the transistor M2 and in this way cuts the PF loop and recovers the initial level of the trigger threshold. This ensures the confluence of the both Schmitt thresholds in one and short time noise immunity determined by NF delay.

III. BASIC RELATIONS FOR THE INPUT STAGE

III.1. Switching mode

Three transfer characteristics of the input stage, where the control current Iref is: 20μA, 110μA, and 260μA, are shown in Fig.4. The point of intersection, of these characteristics, with the line $Vout = \frac{Vdd}{2}$ (parallel with the abscise) is a switching point, where the inverter change its output logical level [4]. In the Fig.4 is traced too the line $Vout = Vin - Vth$. This line divides the linear and saturation working regions of the transistor Mn. It is seen that in the switching point the transistor Mn must work in saturation. This condition can be expressed as:

$$Vin\,max < \frac{Vdd}{2} + Vth \qquad (1)$$

where Vinmax is the maximal value of the input voltage.

The minimal value of the input voltage can be define from the condition that the transistor Mn must work in strong inversion mode:

$$Vin\,min > Vth + \sqrt{\frac{2\,Iref}{Kn}} > Vth + 0.3\,V \qquad (2)$$

In the switching point, in order to ensure a high slope of the transfer characteristic, the transistor Mp must work in saturation. Its parameters will be so much close to the ideal as the ratio W/L is higher and the gate voltage Vgp is lower.

III.2. Analysis with low level of output signal

After the switching of the input circuit its output has low voltage level. Because the circuit is "ratio logic" it is necessary that the voltage of the output to be lower than the threshold voltage of the next stage. For that purpose the ratio (Wn/Ln)/(Wp/Lp) of the next inverter must be chosen sufficiently small.

IV. RESULTS

The proposed circuit was designed and simulated using parameters of VTT 0.8μm BiCMOS technology [5] on power supply voltage Vdd=3.3V.

The W/L ratio of the MOS transistors are:
Wn/Ln = 16/5; Wp/Lp = 150/3; Wref/Lref = 150/3; W1/L1 = 300/3; W2/L2 = 300/3.

The (Wn/Ln)/(Wp/Lp) ratio of the first inverter is (30/3)/(300/3) and for the others -(3/3)/(7.5/3).

The transfer characteristics of the circuit for three control currents (20μA, 110μA, 260μA) are shown in Fig.4.

The results of the Transient analysis of the circuits where are apparently the operation of the positive and negative feedback are shown in Fig.5.

The dependence of the threshold voltage Vth versus the control current Iref is shown in Fig.6. It is evident that this relation is very similar to the linear one.

V. CONCLUSIONS

It was shown that the proposed CMOS Schmitt Trigger with Current Controllable Voltage Threshold and Dynamic Hysteresis has a very good dynamic noise immunity and a good opportunity for control of the input threshold by Iref.

With those advantages, the proposed and studied circuit is considered to be very suitable for various application in analog and analog-to-digital signal processing systems.

REFERENCES

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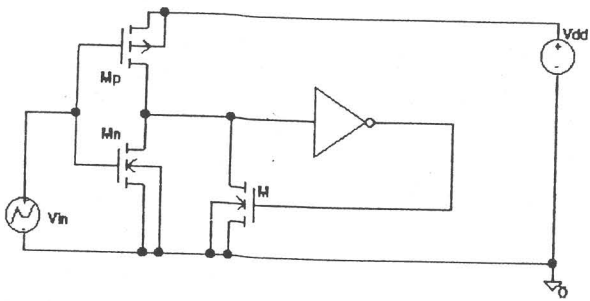

Fig.1. CMOS Schmitt trigger.

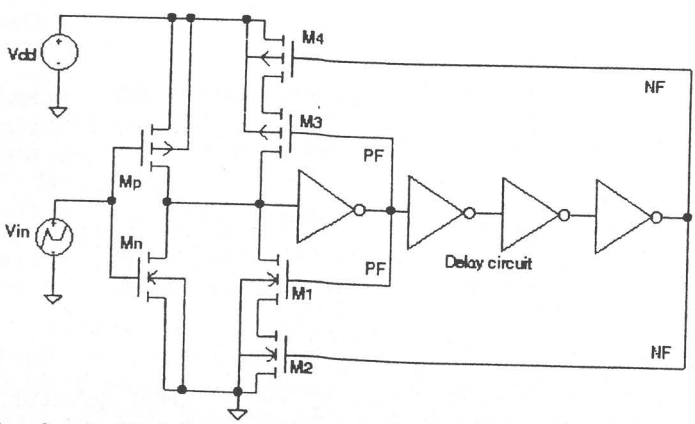

Fig.2. Switching circuits with dynamic hysteresis.

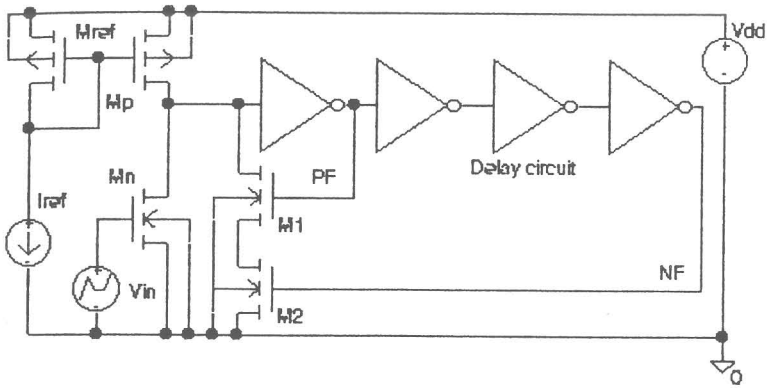

Fig.3. The new circuit.

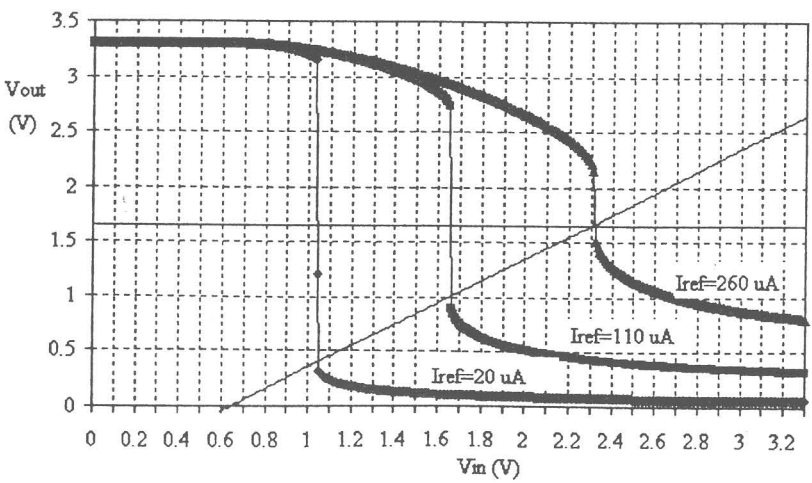

Fig.4. Transfer characteristics

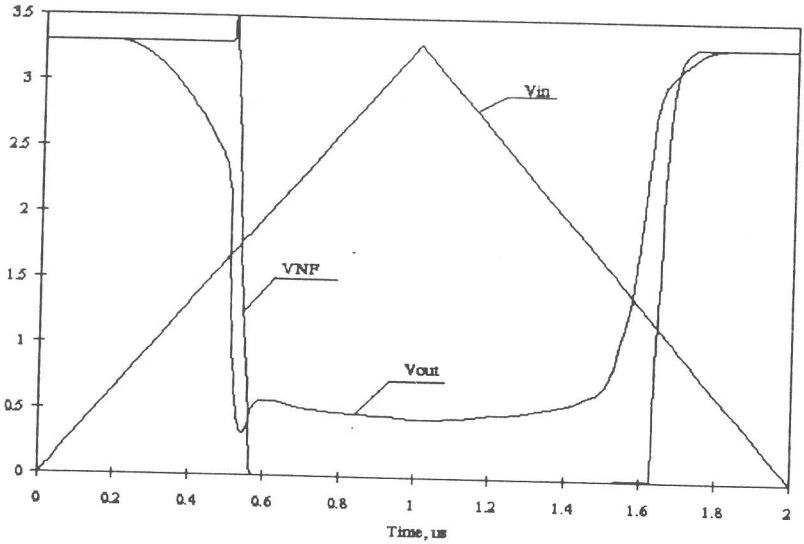

Fig.5. Transient analysis results.

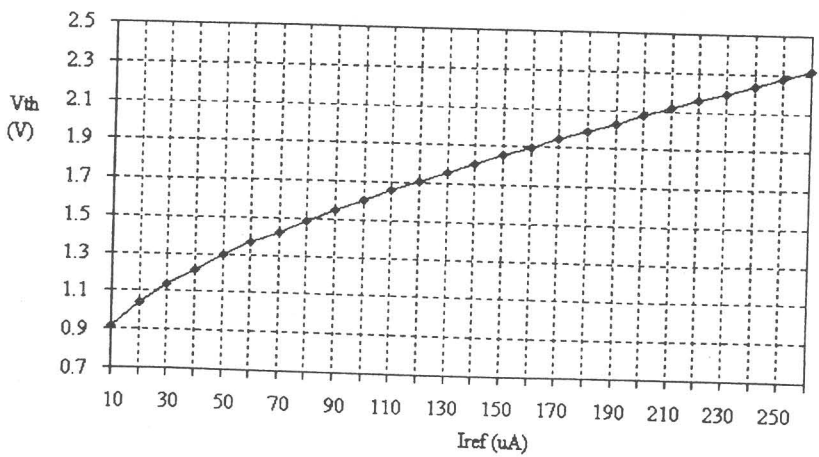

Fig.6. The threshold voltage Vth(V) v/s control current Iref(μA)