Methodology For Custom Analog Monolithic Block Design in CADENCE Environment

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Abstract: *The range of today's microelectronics applications is being shifted towards analog monolithic circuits and mixed analog-digital components. In the same time the analog design methodology has not kept pace with that of digital design. In our case designers had to adopt the limitations imposed by technologies and software tuned for digital applications, and should in some way resemble the human approach to imprecise analogue design problems. We mainly concentrated on the standard and low-cost digital CMOS process and tried to include new analogue domain knowledge and design methods for new analog circuits using the CADENCE software package.*

Here some modifications of flows needed for the realization of a full - custom analog circuit using the CADENCE software are discussed. The well - known "top-down" analogue synthesis approach is used. The complex design tasks are partitioned into smaller sub-problems and resolved separately. Our approach does not imply a change of technology, only a modification of device structures. The more drastic approach asks for additional modifications during the Layout Synthesis and Verification Steps. This excludes standard cell approaches. In the case of CADENCE software it involves manual placement procedures, especially for the input analog stages, choosing an appropriate topology for each building block of the analog circuit, appropriate choice of input - output cells, interactions at the geometry layout level for separating n-wells with different biasing.

To test our concept and implement the approach in a real design we have chosen a precision op. amp. design. Accurate behavioral analyses of the structure are made. It is laid out manually for 2 μm CMOS Nwell ALCATEL Mietec technology.

Introduction

The range of today's microelectronics applications is being shifted towards analog monolithic circuits and mixed analog-digital components. In the same time the analog design methodology has not kept pace with that of digital design. This caused first a worldwide shortage of analog designers and the second an increasing need for CAD synthesis tools for analogue design. It is well known that the design of analog parts of today's monolithic integrated circuits is still done mostly manually and is very time consuming and costly. In our case designers had to adopt the limitations imposed by technologies and software tuned for digital applications, and should in some way resemble the human approach to imprecise analogue design problems.

We mainly concentrated on the standard and low-cost digital CMOS process and tried to include new analogue domain knowledge and design methods for new analog circuits using the CADENCE software package.

Design Flow

It is well known that the CADENCE software package is a general - purpose CAD tool capable of designing digital, mixed and analog circuits. It is well suited for semicustom technology styles. A great variety of standard cells, such as op. amps., comparators, references, etc., pre-designed by experts and organized in cell libraries is available. However, the only way to use performance trade-offs and technology

changes with standard cells is to select the available cells from the library or to change the library, which restricts the flexibility and re-usability of the design.
Here some modifications of flows needed for the realisation of a full - custom analog circuit using the CADENCE software are discussed. The main problems here are connected with the design of custom analog parts using a package tuned for semi-custom digital and mixed applications.
The well - known "top-down" analogue synthesis approach is used. Here complex design tasks are partitioned into smaller sub-problems and resolved separately. The synthesis algorithm performs behavior - to - structure and structure - to - layout phases (Fig. 1) The design of the specific fixed - topology circuit starts from user-requirements and technology parameters. The simulation accuracy depends upon the implemented MOSFET models. In our approach we adapted the used devices to the given circuit topology. It did not imply a change of technology, only a modification of device structures. This is shown as a thicker line between Circuit structure and Devices on Fig. 1. We use a complex MOSFET models (SPICE levels 2), which ensures high accuracy in all MOSFET operating regions.
Next to custom modification of MOSFET's with the given technology, the more drastic approach asks for additional modifications during the Layout Synthesis and Verification Steps. This excludes standard cell approaches. In the case of CADENCE software it involves manual placement procedures, especially for the input analog stages, chosing an appropriate topology for each building block of the analog circuit, appropriate choice of input - output cells, interactions at the geometry layout level for separating n-wells with different biasing. It must be noted that this approach is time-consuming.

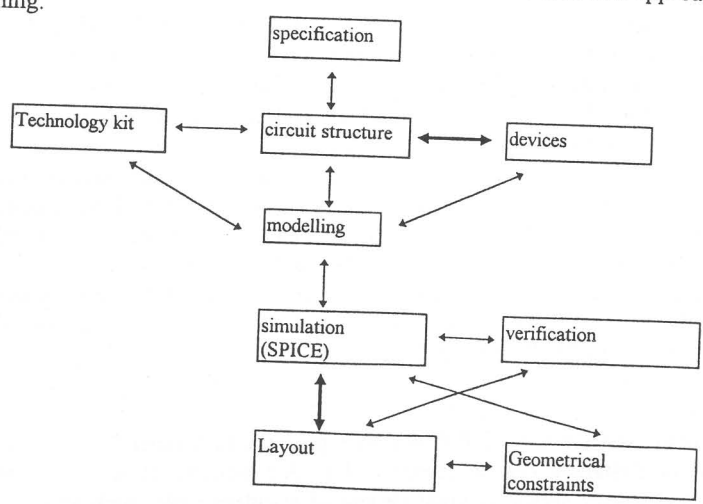

Figure 1: Design Flow chart for full - custom analog design using CADENCE.

Example: Design of a precision CMOS operational amplifier.

To test our concept and implement the approach in a real design we have chosen a precision op. amp. design. The structure needed accurate behavioral analyses as well as to be laid out manually for 2 μm CMOS Nwell ALCATEL Mietec technology.

1. Description of the elementary cells.

The main precision op.amp. parameters are evaluated by the values of their input currents and offset voltage as well as the related temperature coefficients. A sufficiently high voltage gain needs to be maintained. As all the inputs of the precision CMOS op.amp. are MOSFET gates, their input currents have practically zero values. That is why the main cause of the poor precision of the CMOS op.amps. is increasing the input offset voltage U_{io}.

In the chosen op.amp. example two types of measures have been undertaken in order to minimize U_{io} - topology modifications as well as using external pins for zero correction. Assuring the equal parameters of the two input differential branches is one of the most important requirements in precision op.amp. design. The input transistors threshold voltages are to be equal and independent of the applied input voltages. This may be achieved by short-circuiting the sources and the substrates of the input transistors. This means that the p- MOS wells must not be connected to the positive pole of the supply voltage. On the other hand, all the input transistors must be placed in a neighbourhood.

The designed op.amp. circuit is shown on Fig.2. It has a traditional two-stage structure and can easily be included and applied as an op.amp. library cell due to its sufficiently high voltage gain at a low consumption. The input stage has a differential input and a non-symmetric output. It determines the circuit offset voltage. The output stage must ensure a big output voltage amplitude and a high power efficiency at minimal non-linear distortions. This requirement is achieved by a common source transistor stage working in AB - class mode. The circuit controlling this output operation mode is very compact thus minimizing chip size dimensions as well as the consumed supply power. The IRP pin serves to bias the op.amp. An additional zero correction can be made using the OFFS1, OFFS2, CMRR1 and CMRR2 pins in two independent ways: 1/ equilizing the currents in both differential branches by applying an appropriate bias to OFFS1 or OFFS2 inputs; 2/ direct connection of adjustable low-ohmic resistors between the pins named CMRR1, CMRR2 and the positive supply voltage pin.

2. Layout generation.

The design is made using CAD version CADENCE Solaris 9502. There are essentially three groups of cells in the design. One of them consists of the main op.amp. circuit, the second holds the RC - external frequency compensation circuit and the third consists of all I/O cells. The standard cell approach is not possible for the first two groups and requires manual layout of both cells. Models and scaling of the library mie24lib 6.0 are used. The active circuit has a two-row structure and requires manual modifying of the n-wells and manual placement of the input transistor couples. It has to

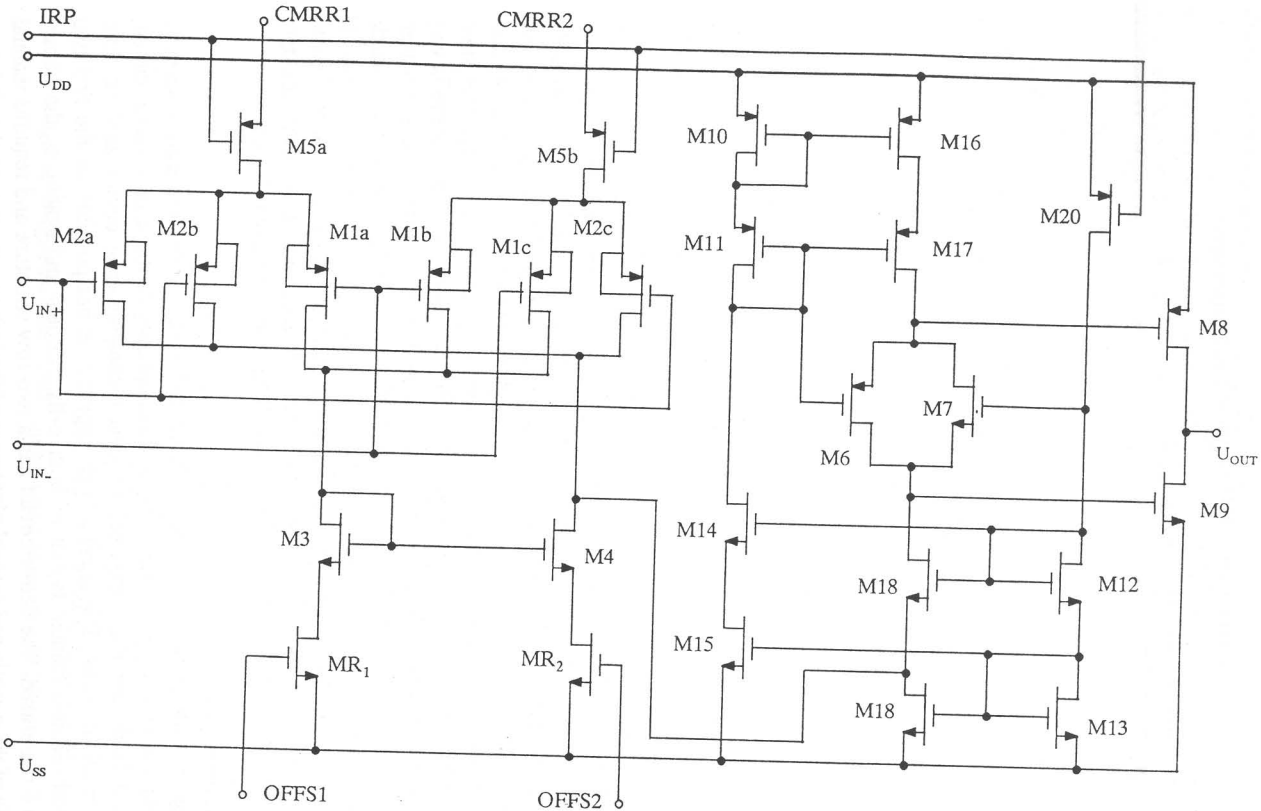

Fig. 2. Schematic of the designed Operational Amplifier

be noted that this part of the design is time consuming. It must be made at a layout level. The chip is not regular at all. For the design verification step the DRC sofware version DIVA 4.3.4 is used. Fig.3 shows the layout generation flow chart used for the precision op.amp. design.

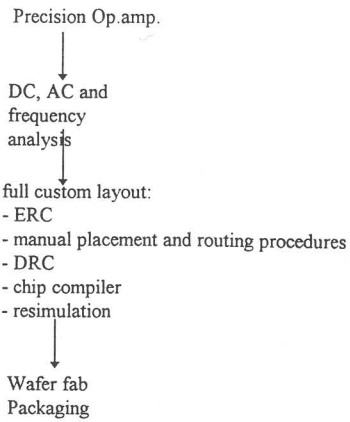

Fig. 3: Layout generation flow chart used for the precision op.amp. design.

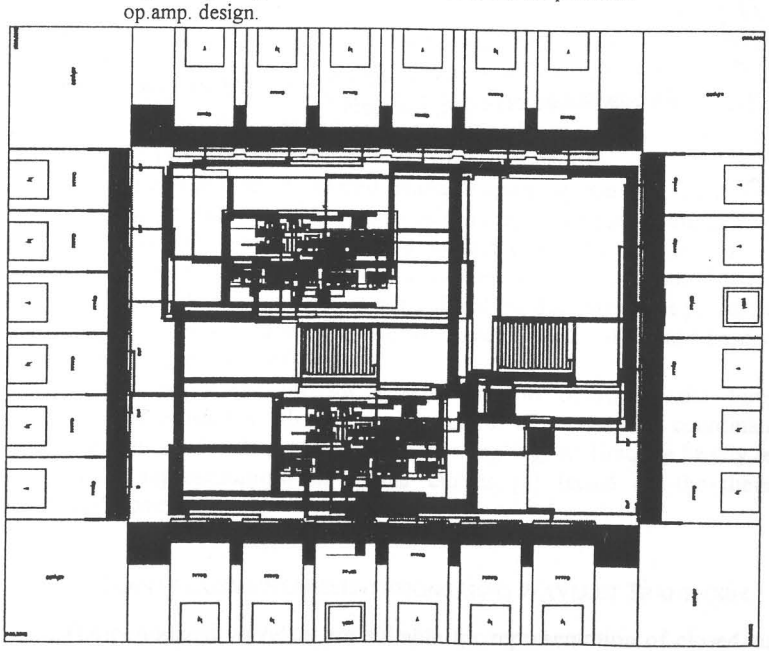

Fig.4: Layout of the produced op.amp. chip

A view of the produced op.amp. chip is shown on Fig. 4. Chip dimensions are 5,4 mm^2 /3.2 x 2.6 mm/. A DIL24 package is used. The essential measurement results of the fabricated structures are the following: Offset voltage V_{OFF} =+2mV; Supply current I_{DD} = 150 μA; Voltage gain A_0 more than 80dB.

Conclusion

In this paper a modification of a standard cell design environment for a full custom analog design is shown. Using this approach a highly integrated circuit is designed and fabricated. However, the full custom layout make the design philosophy more complex and time consuming.

Acknowledgements

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References

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