An accurate pressure-transducer interface for temperatures up to 275 °C

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ABSTRACT

This paper describes a high-temperature pressure-transducer interface for resistive Wheatstone bridges. The long-term drift of the smart sensor, i.e., the (pressure) sensor plus its interface electronics, will be determined by the drift of the sensor element only. A three-signal auto-calibration sequence of the interface electronics keeps the transducer interface virtually free of long-term drift. A novel low-drift pre-amplifier forms an essential element in this system. The high-temperature operation of the transducer interface has been investigated from both an electronic and a packaging point of view. The system has been realized by combining CMOS ASICs with a thick-film packaging technology. The pressure-transducer interface works up to 250 - 275°C with 15-16 bits accuracy.

1. INTRODUCTION

In the oil industry, downhole-pressure measurements are important parameters for oil-reservoir prognosis. The conditions downhole are harsh. The electronic systems have to cope with high temperatures, high pressures, vibration, shock, confined space, etc. In the near future, it is expected that temperatures continue to increase by reason of commercialization of hotter wells which have not been attractive for exploration yet [1]. Improved measurement techniques and long-term monitoring of the well's properties are being required to increase production efficiency. Permanent-installed pressure gauges provide on-line data which allows direct monitoring of the downhole conditions. The long-term stability of these pressure sensors forms their key parameter. Ideally, these sensors should be free of drift because, once installed, maintenance and re-calibration are impossible or extremely expensive.
High-temperature piezo-resistive pressure sensors have been developed that specify a long-term drift of less than 0.01% per year below 125°C to less than 0.15% per year below 300°C [2]. Currently, there is hardly any analog electronic circuitry available that works well at temperatures above 150°C. Moreover, when following the traditional design approaches, the long-term stability of any electronics that would survive at such temperatures would be much worse than specified by the sensor. In this paper, the design of a high-temperature pressure transducer interface will be described that is able to keep up with the specifications of the sensor.
The design of a high-temperature electronic system not only involves the design of the electronics, but also their packaging. Traditionally applied materials such as polyamide, plastics and epoxies are causing long-term reliability problems because they melt, are chemically reacting, or produce aggressive outgassing products. The combination of confined space and sealed environment demands for a reviewing of the currently available packaging technologies. Aspects will be discussed after the design of the pressure-transducer interface.

2. PRESSURE TRANSDUCER INTERFACE

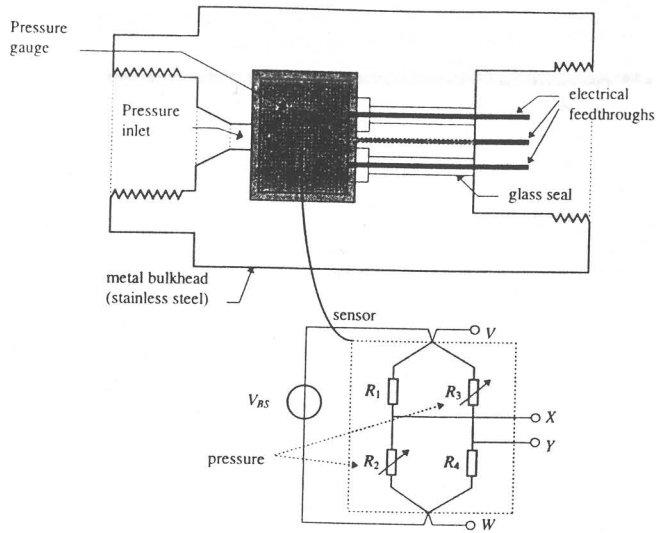

Figure 1 *Cross-sectional view of a pressure-transducer bulkhead. Pressurised well fluid compresses a pressure gauge, which changes the imbalance of a Wheatstone bridge. The electrical schematic of the pressure sensor is depicted to show that this imbalance can be measured by forcing a voltage across the bridge (V_{BS}) while sensing the voltages V_{XY} and V_{VW} according to the four-wire measurement technique.*

2.1 Pressure sensor

Mechanical structures are available that cause changes to the sensor in response to the applied pressure. Figure 1 shows a cross-sectional view of a pressure-transducer bulkhead. Pressurised well-fluid causes a mechanical force to be applied to a resistive pressure gauge. This changes the imbalance of a Wheatstone bridge, where its imbalance is defined as ξ, according to:

$$\text{pressure} \sim \frac{V_{XY}}{V_{VW}} = \xi$$

$$\equiv \frac{R_2}{R_1 + R_2} - \frac{R_4}{R_3 + R_4}$$

Two different types of gauges are available: strain gauges and piezo-resistve gauges. The maximum imbalance ξ_{max} of strain gauges is small, i.e., in the order of 0.5% only, while the maximum imbalance ξ_{max} of piezo-resistive gauges can be in the order of 6%. The imbalance of the Wheatstone bridge can be measured by forcing a supply voltage V_{BS} across the bridge, while sensing the voltages V_{XY} and V_{VW}, respectively. Separate force and sense wires are necessary to eliminate the effects of parasitic wire resistances. The measured imbalance ξ will be obtained digitally in the microcontroller after processing the voltages V_{XY} (the pressure-dependent signal) and V_{VW} (the reference signal) separately.

2.2 Incomplete auto-calibration

The bridge signal is converted to a digital signal by means of a smart signal processor (SSP). Continuous auto-calibration, i.e., periodically measuring the three input signals, is applied to eliminate the effects of long-term drift of the additive and multiplicative errors introduced by the SSP [3,4]. Obviously, the major design aspect of the SSP is that of linearity. The long-term stability of the SSP will then only be determined by the sensor and by the long-term stability of the offset and reference signals. Also note that long-term drift of the microcontroller time-base, i.e., the quantizer step-size, does not affect the long-term stability of the smart sensor. The auto-calibrated conversion of the imbalance ξ of the Wheatstone bridge introduces a dynamic-range problem when both V_{XY} and V_{VW} have to be processed by the same A/D converter. Since the output level of V_{XY} is only a fraction of V_{VW}, the demands for the linearity become hard to be accomplished. Using a pre-amplifier can solve this problem. The bridge-output voltage V_{XY} must be amplified to a level where its dynamic range is in the range of V_{VW}. This however, shifts the dynamic-range problem to a stringent demand for (long-term) stability of the amplifier's gain because the amplifier's gain falls outside the auto-calibration sequence. This can be explained with the aid of Figure 2. The amplifier has been represented by a linear function with offset K and a gain factor G. The A/D converter has also been represented by a linear function with an additive component C and a multiplicative component D, respectively.

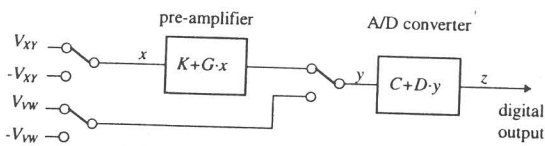

Figure 2. The four-signal auto-calibration applied to the pressure-transducer interface. The microcontroller selects the successive measurement phases.

Since the signal V_{XY} and the reference V_{VW} follow different paths, separate zero measurements are necessary to eliminate the additive components from both the amplifier and the A/D converter. For this reason, the three-signal auto-calibration turns into a four-signal auto-calibration. The zero measurements can be realised by processing the inverted values of the signal and the reference voltages. This can conveniently be implemented with a multiplexer circuit, which causes the bridge-supply voltage V_{BS} to be alternating. The microcontroller can be used to control this multiplexer. So, the digital result M after these four successive measurements becomes:

$$M = \frac{Z(V_{XY}) - Z(-V_{XY})}{Z(V_{VW}) - Z(-V_{VW})} = G\frac{V_{XY}}{V_{VW}} \qquad (2)$$

This result evidently shows the dependency on the amplifier's gain. Consequently, the long-term stability of the SSP is determined by the drift of the sensor as well of the drift of the instrumentation amplifier. This problem can be overcome by the use of dynamic feedback.

2.3 Dynamic-feedback amplifier

The principle schematic of the dynamic-feedback pre-amplifier is shown in Figure 3 [5]. The resistive feedback consists of a chain of K matched resistors. The chain will be made rotating by addressing of the appropriate switches. The feedback is realised by m, n and q resistors,

respectively. Since the resistors are connected as a chain, a resistive load will be present which consists of p resistors. Therefore, it holds that:

$$K \equiv q + m + n + p\,.$$

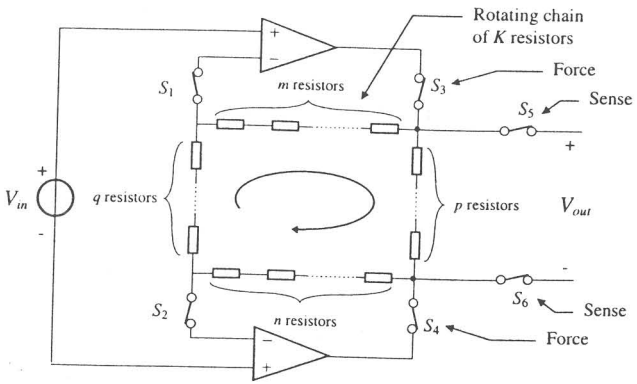

Figure 3 *The principle schematic of a dynamic-feedback instrumentation amplifier. The gain is independent of the ON-resistance of the switches.*

The connections to the two negative input nodes of the opamps are realised by switches S_1 and S_2, respectively. Since these switches do not conduct any current, it follows that the input voltage V_{in} falls across q resistors. Therefore, a current will flow through the feedback that must be delivered by the outputs of the two opamps. As a consequence, switches S_3 and S_4 conduct a signal dependent current. The voltage drop across these switches introduces a nonlinearity, which can be overcome by sensing at the resistor chain by means of switches S_5 and S_6.

The feedback is made dynamic by rotating the resistor chain between the two opamps. Therefore, the feedback has K states. So, a resistor that is part of the load will become part of the feedback later. For this reason, this load resistor is of vital importance for the functionality of the dynamic feedback. The average gain $\overline{G}$ of this amplifier over K successive states is equal to:

$$\overline{G} = 1 + \frac{m+n}{q}\,. \qquad (4$$

Any mismatches between the resistors hardly affects the average gain because there is a compensating effect when the resistors move along the chain. For instance, when all resistors are equal except for one resistor that is a little bit too large, then the gain will be a little bit too large, i.e., larger than described by Eq. (4), during $m + n$ states. During p states, the gain will be exactly according to Eq. (4). However, the gain will be a little bit too small during q states. As a result, there is compensation of all gain errors such that the mismatches appear as second-order effects in the average gain. Drift of the resistors does not affect the average gain at all because rotational speed of the resistor chain is relatively fast, i.e., several kHz.

The resistor chain is controlled by a digital-state machine, which addresses the appropriate switches. Every successive state, the chain rotates one position. So, the number of states is equal to the number of resistors in the chain. Note that the simplest configuration consists of a

chain with four resistors, i.e., $q = m = n = p = 1$. The control of the resistor chain requires that there are 6 switches connected to a single point between every two resistors. Two of these switches are necessary to connect to the negative-input nodes of the opamps and two switches are necessary to connect to the output nodes of the opamps. The remaining two switches are necessary to sense the output voltage across the load resistor(s). Consequently, a total of $6K$ switches is required to realise the dynamic feedback.

2.4 High-temperature electronics

The pressure-transducer SSP has been realised as an ASIC [6,7]. The interface consists of two dynamic-feedback amplifiers to handle signals from strain gauges and piezo-resistive gauges. When handling the signals from piezo-resistive gauges, the second dynamic-feedback amplifier will be bypassed and powered-down. The ASIC also contains a linear VCO to convert the signal, reference and two offset voltages, i.e., the inverted signal and the inverted reference signal, according to Eq. (2). The resulting period-modulated signals will be handled by the microcontroller. The ASIC also contains logic circuitry to control the successive measurement phases.

The design accounts for degradation mechanisms that may impede the ASIC's reliability at high ambient temperatures. These are, among others, corrosion, electromigration, diffusion, mechanical stresses, leakage currents and latch-up. The package-related issues are discussed in the next section. Electromigration problems have been solved by increasing the widths of the aluminium interconnection patterns, while the use of redundant contacts and vias further reduces this problem. Furthermore, the circuit has been designed to be low-power. On the other hand, the biasing currents should be large enough to overshadow high-temperature leakage currents. Otherwise, these leakage currents may cause total runaway of the biasing. For high-temperature applications, a CMOS technology is preferred above the bipolar technology because leakage currents only affect the biasing conditions of the circuit but do not alter the device characteristics significantly. MOS devices have shown to be functional up to 350°C, whereas bipolar transistors are hardly useful above 225°C. Moreover, the implementation of the required logic circuitry and switches is much simpler in a CMOS technology. Latch-up can be obviated by guarding, and by keeping sufficient distance between NMOS and PMOS sections.

3. ASIC RELIABILITY AND PACKAGING DESIGN CONSTRAINTS

When a high-temperature electronic system is developed, it is essential to investigate also the behaviour and properties of the packaging. The reliability of a high-temperature electronic system is influenced by the chemical and mechanical properties of all components inside the packaged module. In an oil well, all electronics will be hermetically sealed in a confined space. Therefore, the used materials should be well chosen. Since the ASIC designs are realised in silicon, most mechanical and chemical aspects are related to the properties of silicon. The main degradation mechanisms that may impede the ASIC's reliability at high ambient temperatures arise from corrosion, electromigration, diffusion, mechanical stresses, leakage currents and latch-up. Since the first three effects are related to the aluminium metal system, special attention has to be paid to the metal system.

3.1 ASIC reliability using an aluminium metal system

Corrosion of aluminium can easily be avoided by removing all oxygen during packaging of the ASIC. The package should be hermetically sealed under a chemically inert gas, e.g., nitrogen. Electromigration becomes a serious problem when the current densities in the

aluminium conductor patterns are roughly exceeding $0.1 mA/\mu m^2$. Altering the metal system for, for instance, tungsten can develop an electromigration-hardened process. This adds costs plus that such processes are not widely available. Therefore, for the pressure-transducer interface, there has been chosen to trade silicon area to allow for increased widths of the aluminium interconnection patterns. Moreover, using multiple contacts and vias further reduces this problem as it adds redundancy. Furthermore, the circuits must be designed low-power. This is strongly dependent on the application, but in the case of the pressure-transducer interface, this is well achievable, as the ASIC's current consumption stays below 5mA. The third effect is that silicon tends to diffuse into pure aluminium. This process is accelerated at higher temperatures. Therefore, a diffusion barrier would be required at the interfaces where the on-chip devices, e.g., transistors, diffused resistors and junction capacitors, are contacted with the aluminium conductor pattern. A very simple, though effective, solution to eliminate these diffusion problems is to add 1% silicon to the aluminium on beforehand. The alloy aluminium-silicon (1%-Si, 99%-Al) does not use up any silicon before 500°C. At 300°C, the chemical equilibrium lies around 0.5% silicon, so sufficient overkill is present to avoid any detrimental diffusion effects. This technique is commonly applied in commercially available CMOS processes. Also note that aluminium for wire bonding also contains 1% silicon in order to obtain wire strengths comparable to gold. In conclusion, it is possible to obtain reliable high-temperature electronics from standard CMOS technologies using aluminium as a metal system.

3.2 Mechanical considerations

Mechanical stresses can arise from differences of thermal expansion of the different materials, which may lead to fractures. Shocks and vibration have their impact on devices, especially when their connection area is small with respect to their mass.
The thermal expansion coefficients of the ceramic substrates and packages must be matched to the one of silicon ($2.6 \times 10^{-6}\ °C^{-1}$) to avoid ASIC fracture. The ASIC-bonding will have to be elastic to cope with thermal strain. For this reason, it is to be avoided to use polyamide as a carrier material because it expands much faster with temperature than ceramics. Metal packages must be Kovar-based because the temperature-coefficient of Kovar is matched to the one of silicon.

3.3 Chemical considerations

Often, reliability problems arise from outgassing of components. The resulting chemical attack causes corrosion or causes formation of compounds. Eventually, this leads to reliability problems. Corrosion is accelerated by temperature while moisture acts as a catalyst. Therefore, when sealing an electrical component's package, it should be done in an environment filled with a chemically inert gas, e.g., nitrogen (N_2). Making all components more robust against chemical attack does not solve the problem of outgassing at all. Such materials must be avoided completely. Due to the sealed environment, some reactive gasses may cause failures otherwise. Moreover, it is always recommended to place any circuitry in a high temperature vacuum to remove all outgassing prior to filling the package with nitrogen or helium. This "vacuum-baking" step covers a main part of the burn-in of the tool.

4. HIGH-TEMPERATURE PACKAGING OF THE PRESSURE-TRANSDUCER INTERFACE

In order to design a temperature-resistant package, it is necessary to identify the different components inside these packaged modules. It will be assumed to package a hybrid circuit

according to the thick-film technology [8]. The packaging of single ASICs then follows from simplifications of this technique. Five levels can be distinguished:

I. Die bonding, i.e., the connection of the ASIC to the substrate.
II. Wire bonding forms a connection between the ASIC's bondpads and the interconnection patterns. Wire bonds are also necessary between the interconnection patterns and the package leads, i.e., the posts.
III. Chip to conductor. Components that are small in size, e.g., ceramic chip capacitors, chip resistors, diodes, etc., will be directly soldered onto the interconnection patterns.
IV. Conductor pattern to substrate, i.e., the printing of interconnections, resistors and small capacitors.
V. Substrate to package cavity, i.e., the connection of the substrate to the package cavity. Note that the package itself may be viewed upon as a small chassis. It usually is a given unit using well-specified materials, e.g. ceramics or stainless steel.

These levels have been depicted in Figure 4 and will be closer analysed in the following sub-sections.

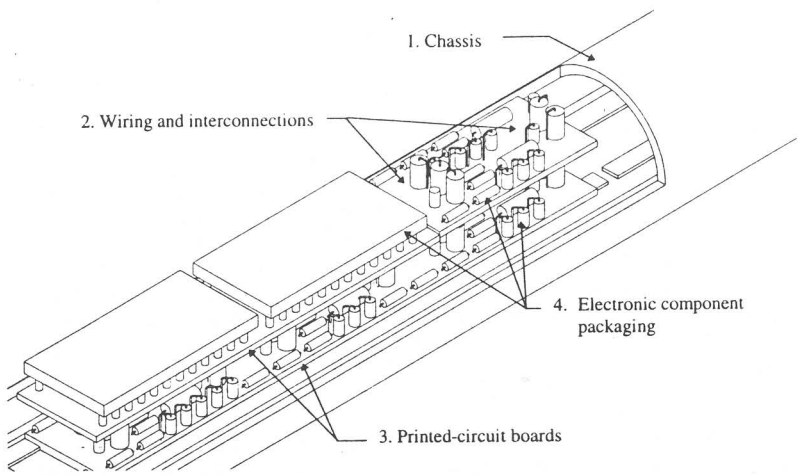

Figure 4. The five electronic-component packaging levels.

4.1 Die bonding

The ASIC must be bonded to a substrate, which usually is, i.e., for high-temperature purposes, a gold-plated area on top of a ceramic substrate. Elastic bonds are a prerequisite to avoid mechanical stresses between the substrate and the silicon. Two types of die-bonds are suitable for high-temperature applications: Eutectic bonds and high-temperature epoxy bonds: The well-known silicon-gold eutectic bond [9], which consists of 6%-94% Si-Au and has a melting temperature of 370°C. The resulting bond has a high elastic modulus and provides a good electrical contact to the backside of the ASIC.

As compared to other bonds, the eutectic bond is favourable as it forms a perfect medium between the silicon ASIC and the gold-plated carrier material. Latch-up susceptibility will be greatly reduced by electrically contacting the backside of the ASIC. Furthermore, the eutectic

bond provides an excellent thermal contact to the on-chip devices which results in junction temperatures that are close to the ambient temperature.

4.2 Wire bonding

Thin wires are used to form connections between ASICs, substrates and package posts. Long bonding wires show wire sweep due to shocks and vibration. They can cause shorts to neighboring wires or even come off. Therefore, short bonding wires are necessary. Commonly used bonding wires are made from gold or aluminum.

Wire bonding with gold will cause problems at high temperatures because aluminum of the ASIC's bondpads diffuses into the gold wire. The resulting compound is called purple plague because of its purple color. This process is further accelerated due to the presence of silicon which acts as a catalyst. As the gold consumes the aluminium film, the compound film loses adhesion to the oxide or silicide underneath. This causes the bond wire to be torn loose. Therefore, to prevent the occurrence of purple plague, aluminium bonding is recommended [10]. Aluminium is more susceptible to corrosion, but when the atmosphere consists of dry nitrogen then it is not expected to give any problems.

Ceramic packages and substrates make use of gold-plated bonding areas. The Kovar posts, i.e., the connection to the inner leads of the package are also gold-plated. When using aluminium wires in stead of gold, it may be expected that the purple-plague problem will be transferred from the ASIC to the gold-plated bonding areas. Fortunately, this is hardly the case. The aluminium film on the ASIC is only 1 - 2μm thick while the bonding wire has 25μm - 50μm diameter. Therefore, a gold wire would consume this thin aluminium film easily. On the contrary, an aluminium wire will not be consumed by the gold film (of approximately 10μm thickness) at the posts or bonding areas so easily because the gold film does not have enough volume to consume a significant part of the aluminium wire. Nevertheless, due to the presence of both gold and aluminium, it is expected to see some purple-plague formation. This has been verified by measurements. It was found from aluminium wires (32μm-diameter) bonded to gold-plated conductor patterns of 10μm thickness that there was light-brown coloration around the bond after 528 hours at 300°C. Wire-pull tests showed approximately 50% loss of strength. After 528 hours, the average measured pull-strength equals 4.36 grams, which is still above the military specified value of 3 grams. Therefore, all ASIC bondpads must be bonded by using aluminium wires. All remaining bonds have to be completed by gold wires, i.e., the connections between the posts and the substrates. A cross-sectional view of a package where these techniques have been applied is shown in Figure 5.

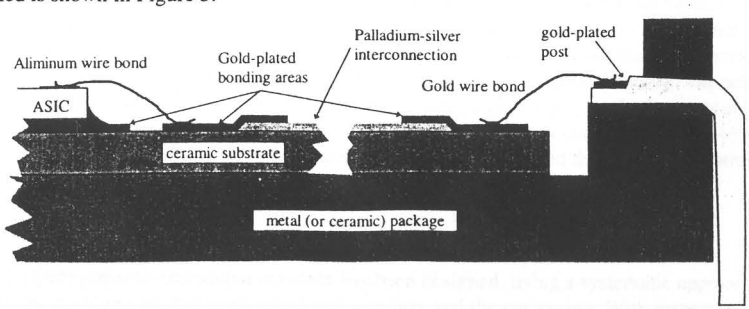

Figure 5 Cross-sectional view (not to scale) of a high-temperature package. Both aluminium and gold wire bonds will be present throughout the package.

4.3 Substrates

The choice of the substrate depends on the thermal expansion coefficient between silicon and substrate. A value close to the one of silicon (2.6×10^{-6}/°C) is mandatory to avoid chip fracture. A commonly used material is the ceramic material alumina (Al_2O_3), which is a very good electrical insulator and well suited for high-temperature applications.

4.4 Interconnection and wiring of components

The interconnection patterns on alumina substrates are made of precious metal palladium-silver. Wire bonding to the palladium-silver tracks is difficult. Therefore, as was shown in Figure 5 already, gold-plated bonding areas are necessary. These areas generally are 0.5mm × 2mm × 10µm gold areas with 1mm overlap over the palladium-silver tracks.

4.5 Hybrid and ASIC packaging

Two types of material for high-temperature packages can be distinguished: metal and ceramics. The electrical feedthroughs of metal (Kovar-based) packages are isolated from each other by glass encapsulations. The Kovar-based feedthroughs have gold-plated connection areas as was shown in Figure 5 already. Hybrid circuits use an alumina substrate that will be attached in a similar way to the cavity of a metal flat-pack. The substrate is pressed into an epoxy paste and cured at a temperature below 300°C in order not to impair the bonding quality of the ASICs, chip resistors, capacitors, etc. Ceramic packages are merely used to package individual ASICs. ASICs can be directly attached to the cavity using an epoxy paste or by means of an eutectic bond because the cavity is gold-plated. Care should be taken to use fritless feedthroughs as side-brazed pins might fall apart at high temperatures.

4.6 Printed-circuit boards

At present, PCBs are usually made of epoxy or polyamide. Both are synthetic materials. Epoxy cannot be used at high ambient temperatures because it simply burns away above 175°C. Polyamide is more temperature resistant, but will be abandoned because of its large thermal-expansion coefficient, i.e., approximately 45×10^{-6} °C^{-1}, which results in mechanical stresses. For example, there will be friction at the solder joints when the temperature is cycled. Moreover, the conductive interconnection patterns adhere much more firmly to alumina than to polyamide. Therefore, the highest reliability is to be expected from using alumina printed-circuit boards.

5. THE PACKAGED PRESSURE-TRANSDUCER INTERFACE

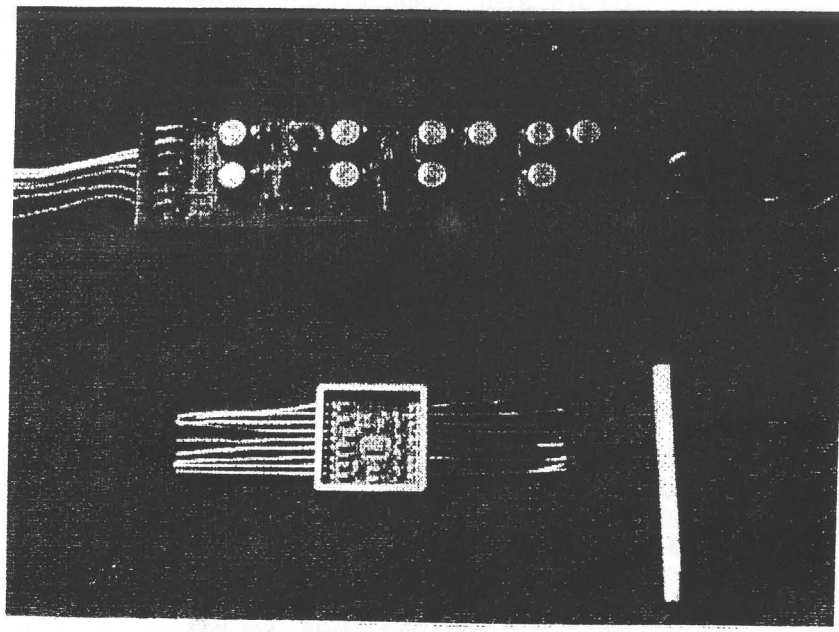

Figure 6 *The pressure-transducer interface in a high-temperature package. The old PCB-version (175°C) has been shown for comparison. The matchstick indicates the size of the old and new circuits.*

Figure 6 shows a picture of the pressure-transducer interface where all high-temperature packaging techniques as described in the previous section have been applied. A matchstick has been shown as a figure of merit. The upper printed-circuit board is the old version, which was functional up to 175°C. A metal package has been used which contains an alumina thick-film substrate. The die bonding in this prototype has been realised by means of an epoxy paste because a thick oxide at the ASIC's backside did not allow for eutectic bonding. The wire bonding at the ASIC has been realised by means of aluminium wires, while the posts are connected to the substrate by means of gold wires. This circuit has been successfully tested for 3 weeks at 225°C where other components in the system limited the maximum testing temperature. Brief tests [11] proved that the circuits are functional up to 275°C.

6. CONCLUSIONS

An accurate pressure-transducer interface has been designed, using a systematic approach to solve the problems related to the electronic circuitry and the packaging. With respect to the electronic circuitry it has been shown that CMOS technology is more suited than bipolar technology. At the chip level, measures such as guarding have been taken to obviate latch-up

phenomena. Usually, biasing currents of about 10μA per component are large enough to overshadow the effects of leakage currents, for temperatures up to 250 °C.
An excellent long-term stability of the interface is obtained by applying the concepts of continuous auto-calibration and dynamic feedback of the pre-amplifiers.The packaging related problems have been discussed and recommendations have been given regarding the diebond, the wire bonding, the ASIC packaging and the applied printed circuit boards. A complete interface has been built and shows good test results for temperatures up to 275 °C.

7. ACKNOWLEDGEMENTS

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