# A 'MODULO N+1/2 DIVIDER'

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*Summary: As called 'modulo N+1/2 divider' produces some frequency $f_O$ from input frequency $f_I$ by the equation $f_O = f_I/(N+1/2)$. The most disadvantage of the simplest 'modulo N+1/2 divider' has been analysed in this paper. The main divisor is toggled whit a twice higher frequency $2f_I$ than the input frequency $f_I$. The idea of the offered in this paper 'modulo N+1/2 divider' consist of modification the known device so that the main divisor to be clocking by a lower frequency. The device contains a main divisor with a division factor equal to N+1 and an additional divisor on 2. The additional divisor controls an EOR gate that changes the toggling edge of the frequency at the input of the main divisor. A work analysis of the offered 'modulo N+1/2 divider' has been made. The deviation of the output frequency period has been analysed as well as the dynamic power dissipation. Some limits about device parameters and input frequency has been pointed. The most advantage of the offered device is the lower toggling frequency for the main divisor causing a reduction of the dynamic power dissipation.*

## I. INTRODUCTION

As called 'modulo $M$ divider' produces some frequency $f_O$ from input frequency $f_I$ by the equation $f_O = f_I/M$. Some times the factor $M$ is not whole number. More often $M = N+1/2$. This kind of divisor where the division factor is equal to $N+1/2$ is called 'modulo $N+1/2$ divider'.

One way to realize some kind of 'modulo $N+1/2$ divider' is to use a rate multiplier like '4089, '4527 e.t.c. This solution is not recommended because the rate multipliers produce output sequences skipping some pulses from the input sequence. Thus causes that the output sequences are irregular.

One another way of 'modulo $N+1/2$ divider' realizing is to use a Phase Locked Loop (PLL) or Frequency Locked Loop (FLL), but this way is very complex and it is recommended for using when the factor M is more complicated.

Shown on fig. 1 device is the simplest solution of realizing a 'modulo $N+1/2$ divider'. It contains an additional multiplier by $2$ before the main divider which factor of division is $2N+1$. The additional multiplier could be realized by an EOR gate and an inverter used as a delay chain.

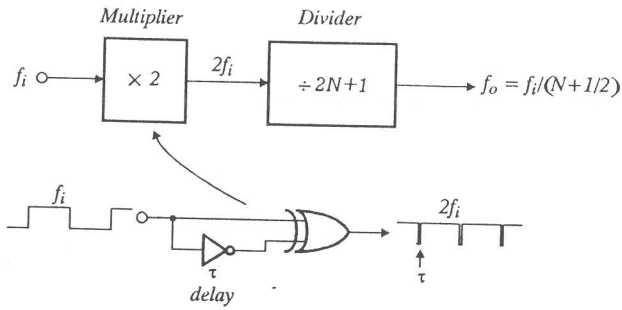


**Fig. 1. The simplest 'modulo N+1/2 divider'**

However, there exists one general disadvantage. The main devider is toggling whit a twice higher frequency $2f_i$ than the input frequency $f_i$. Thus causes a higher dynamic power dissipation when the device is built on CMOS logic.

## II. A 'MODULO N+1/2 DIVIDER' WITH A LOWER CLOCKING FREQUENCY

The idea of the new offered device is to modify known device so that the main divider to be clocking by a lower frequency and where the dynamic power dissipation would be reduced. The offered device is shown on fig. 2. This device contains a main divider whit a division factor equal to $N+1$ and an additional divider by 2. The additional divider controls an EOR gate that changes the toggling edge of the input frequency.

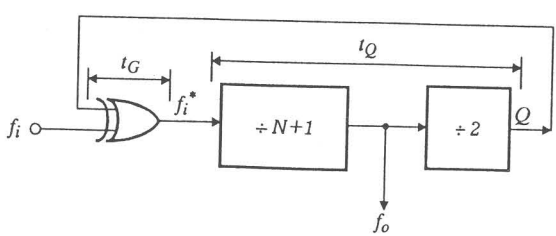


**Fig. 2. A modification of the 'modulo N+1 divider' with a lower clocking frequency.**

The operation of this device is shown on fig. 3. In fact, the EOR gate adds one toggling edge each period of the output frequency. In each period of fo the toggling edges are changing. The main divider is clocking approximately

by the same frequency as the input frequency.

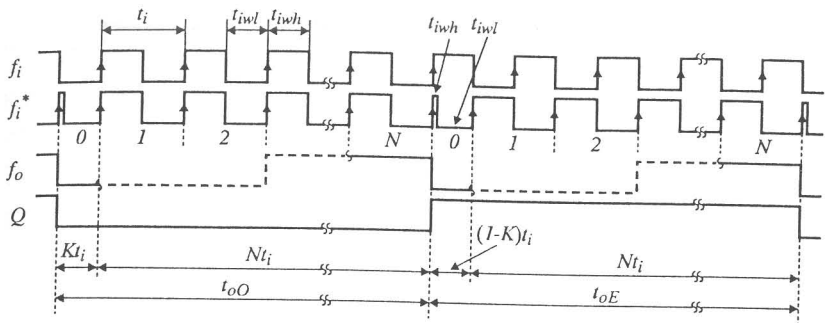


**Fig. 3. The timing diagram of the offered 'modulo N+1/2 divider'.**

The meanings of the using symbols are:

$t_{oO}$ — odd periods of the output frequency;

$t_{oE}$ — even periods of the output frequency;

$t_o$ — middle value of the output frequency;

$\delta t_o$ — $t_o$ deviation;

$K$ — duty cycle of the input frequency.

Using diagrams, it can be determined:

$$t_o = \frac{t_{oO} + t_{oE}}{2} = \frac{Nt_i + Kt_i + Nt_i + (1-K)t_i}{2} = \left(N + 1/2\right)t_i,$$

$$\delta t_o = \frac{t_{oE} - t_{oO}}{t_o} = \frac{Nt_i + Kt_i - Nt_i - t_i + Kt_i}{\left(N + 1/2\right)t_i},$$

$$\delta t_o = 2\frac{K - 1/2}{N + 1/2}. \qquad (1)$$

If $K = 1/2$, then $\delta t_o = 0$.

If $K_{min} \to 0$, then $\delta t_{o\,min} \to \frac{1}{N + 1/2}$.

If $K_{max} \to 1$, then $\delta t_{o\,max} \to \frac{1}{N + 1/2}$.

As can be seen from equation behigh, if the factor of the duty cycle of the input frequency is *1/2*, the deviation of the output frequency is close to zero.

The base device contains one main divider with a factor of division

$2N+1$. The offered device contains one main divider with a factor of division $N+1$ and one additional divider by 2. The whole factor of division is $2N+2$. So, it can be considered that both factors are approximately equal and that both devices contain dividers with an approximately equal complexity. That means that both devices would be built by the same number of flip-flops.

The dynamic power dissipation for the dividers built on CMOS is done by the following equation:

$$P_D = \kappa f \frac{M-1}{M},$$

where $\kappa$ is a factor of proportionality, $f$ is the toggling frequency, $M$ is the module of division. For the base device $P_D = \kappa 2 f_i \frac{2N}{2N+1}$ and for the offered device $P_D{}^* = \kappa f_i{}^* \frac{2N+1}{2N+2}$. As far as $f_i{}^* = \frac{f_o}{N+1} = \frac{\left(N+1/2\right)}{N+1} = \frac{2N+1}{2N+2} f_i$ $P_D{}^* = \kappa f_i{}^* \frac{(2N+1)^2}{(2N+2)^2}$. Then:

$$\frac{P_D{}^*}{P_D} = \frac{1}{2} \frac{(2N+1)^3}{(2N+2)^2 2N} \tag{2}$$

The minimum value of $N$ is 1. Then $\frac{P_D{}^*}{P_D} = \frac{1}{2} 0.84$. If $N$ grows up, the relation between $P_D{}^*$ and $P_D$ becomes close to 1/2. So, it can be considered that the offered device has a dynamic power dissipation approximately twice lower than the base device.

There exist some limitations using the offered 'modulo $N+1/2$ divider'. The width of the additional pulse $t_{wh}$ is:

$t_{wh} = t_G + t_Q$, where $t_G$ is the propagation delay time of the EOR gate, $t_Q$ is the propagation delay time of the dividers. The pulse $t_{wh}$ has to be larger than the minimum pulse width $t_w$ required by the main divider, e.g.:

$$t_G + t_Q \geq t_w \tag{3}$$

Some additional limitations could be determined by the timing diagrams of the offered device:

$$t_{iwh} \geq t_G + t_Q - \left(1/f_{max} - t_w\right), \; t_{iwl} \geq t_G + t_Q - \left(1/f_{max} - t_w\right), \tag{4}$$

where $f_{max}$ is the maximum freguency for the main divider. So, It can be considered that the period of the imput signal has to be $t_i \geq 2\left(t_G + t_Q - t_w + 1/f_{max}\right)$ and when $t_G + t_Q = t_w$ the maximum input

frequency is close to $f_{max}/2$.

### III. AN EXAMPLE

Let it is necessary to generate a 153.6 kHz frequency for a bode rate generator (9600 x 16 = 153600). Let this frequency has to be produced from a stable base frequency 1 MHz as shown on fig. 4. A divider with a factor of division 6.5 could be used for this purpose ( 1000000/6.5 = 153846 ).

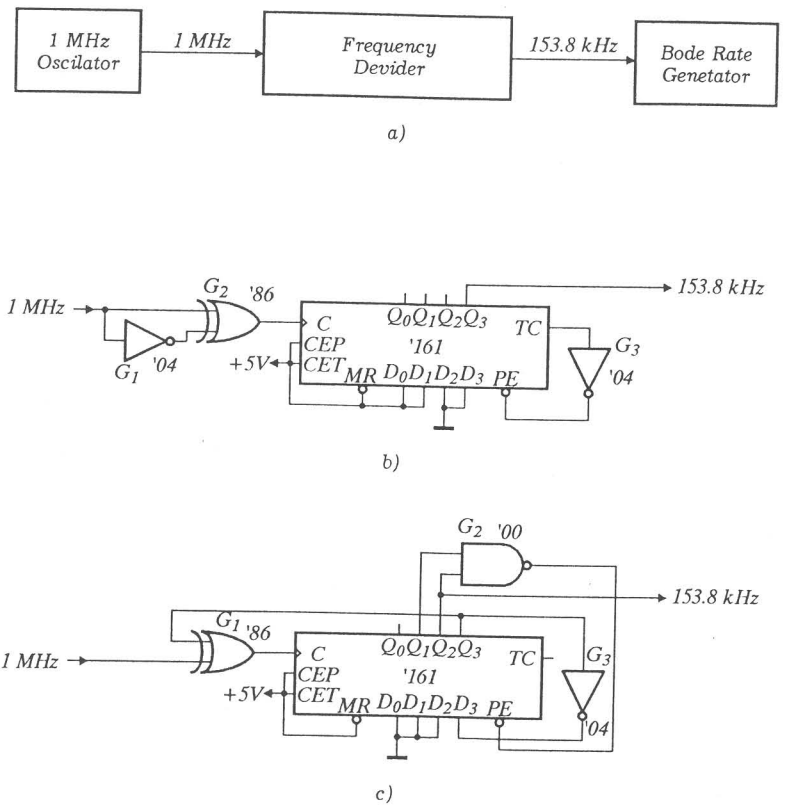


**Fig. 4. A 'modulo 6+1/2 divider' applying: a) — block diagram; b) — a devider built by the base device; c) — a devider built by the offered device.**

Fig. 4.a shows receiving of 153.8 kHz from 1 MHz using 'modulo *N+1/2* divider' where the number *N* is 6. Fig. 4.b shows a module 6.5 divider that uses

the base device. The additional multiplier by *2* is realized by the inverter $G_1$ and the EOR gate $G_2$. The main divider by *13* is built using a counter '161 that counts from 3 to 15.

Fig. 4.c shows the same module 6.5 divider, but now it is built by the offered device. It uses the same elements. The main divider by 7 is composed by the first three flip-flops of the counter '161. The NAND $G_2$ is a detector of state 6 that loads the main divider with zero. The fourth (most significant) flip-flop forms with the inverter $G_3$ the additional divider by *2*. Each time when the counter '161 is loading the state of the fourth flip-flop is inverting.

## IV. CONCLUSIONS

The most disadvantage of the simplest 'modulo *N+1/2* divider' has been analysed in this paper. The main divisor is toggled whit a twice higher frequency $2f_i$ than the input frequency $f_i$. Thus causes a rising of the power supply consumption when the device is built by CMOS.

A modification of analyzed 'modulo *N+1/2* divider' has been offered in which the main divisor is clocking by a lower frequency. The device contains a main divisor whit a division factor equal to *N+1* and an additional divisor on *2*. The additional divisor controls an EOR gate that changes the toggling edge of the frequency at the input of the main divisor.

A work analysis of the offered 'modulo *N+1/2* divider' has been made. The deviation of the output frequency period has been analysed as well as the power supply consumption. Some limits about device parameters and input frequency has been pointed.

The most advantage of the offered device is the lower toggling frequency for the main divisor. As far as the dynamic power dissipation in CMOS depends proportionality from the toggling frequency, the dynamic power dissipation of the offered device is decreased in comparison of the base device.

## V. REFERENCES

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