Heat-Resistance Estimation of Digital Hybrid Integrated Circuits

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INTRODUCTION:

Up-to date electronics includes as more as possible digital integrated circuits One of the integrated circuits qualitative indices are their temperature resistance.

It defines capability for keeping the most important electrical characteristics' values into defined limits during high and lower temperature influences. The heat - resistance of the IC is their estimation at positives' temperatures. The most frequently used estimations of are temperature dependence of signal time delay and output voltage low and high logical levels.

The main reasons for environment temperature influence over the IC dynamic limits are:

* the disagreements of the DIC's different components temperature coefficients of linear extension;
* the rise of mechanical strain;
* the lose of hermetically;
* the pressure into the contacts;
* bad metalisation adhesion;
* dislocations and defects into the chip which cause current gain drift.

It has be known that for endurance limit's resistance during the exploitation it has to do influences and a long burn-in. An electrical characteristic's control at normal temperature for heat - endurance has be made after that. Great loose of time and high price specialised apparatus can not afford using of that methods for incoming control.

The basic aim of that method is to allow individual verification of temperature endurance during DIC's incoming control. Thai is a firm guarantee for higher reliability of electronic systems that includes passing that sort of tests IC.

2. USING CVS METHOD FOR IC HEAT ENDURANCE ESTIMATION.

The essence of that method finds expression in decreasing supply voltage under the nominal value until the first fault appeared at the output of a working IC.

A maximum CVS level corresponds to an anomaly IC. The anomaly CVS testify to presence of some small but essential defects even the IC has not be upheld the whole test. These defects conduct IC's potential unreliability. That kind of defects is source as usual so unsteady inconstant) faults. To find out the reasons of that fault into large and compound IC very often is a quite hard problem.

To be realised the CVS methods for DHIC heat endurance first have be measured CVS of every circuit at the normal environment. Then CVS after cyclical temperature influences (-20 ^{0}C - +55 ^{0}C) everyone determinate time intervals have be measured. Some experiments with digital IC and HIC for proving the CVS' have be made.

3. EXPERIMENTAL RESULTS

Making experiments it has be found that five cyclical temperatures are quite sufficiency for hidden faults detecting. Faults into circuits it has be behaved provocatively be artificially.

Reversible (curve 2) and irreversible changes of critical voltage supply were appear (curve 1) as a result of measurements (fig.4).The dynamic of CVS changes analyse (curve 1) shows that the temperature test has been short. The curve 1 does not establish into the starting position. Fig. 1 and fig.2 include measured results of two batches consisting from 20 circuits.

Fig.3 gives CVS variations for one IC at different time of tests, where:

1- before cyclical temperature influence,

2- after making 5 cyclical temperature tests and

3- after making 150 hours electrical test.

The tests of another batch's IC demonstrate their limit's stabilisation reached (curve 2). CVS changes did not notice into about 20% of all tested circuits from that batch.

4. CONCLUSIONS

Heat resistance estimations of digital IC though varying critical voltage supply of each circuit in flop state and then after influence of five cycles of the temperature have be accomplished. The essence of the method finds expression in supply voltage decreasing from one nominal value to the level it the first fault detected on circuit's output while a coming test was applying.

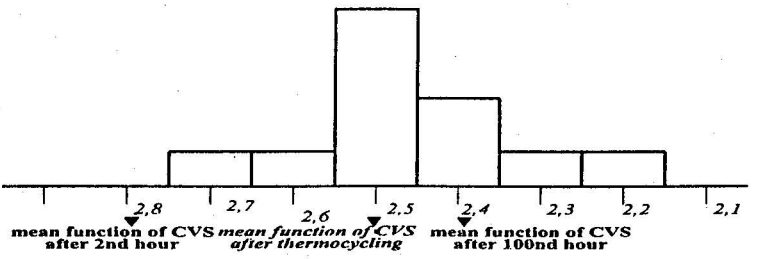

Fig.1. Distribution of the CVS after thermocycling for the 2nd batch on Fig.4.

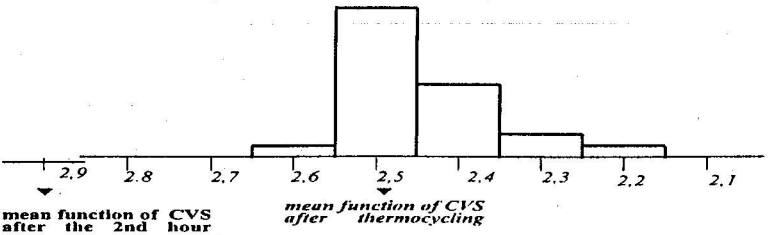

Fig.2.. Distribution of the CVS after thermocycling for the 1st- batch on Fig3.

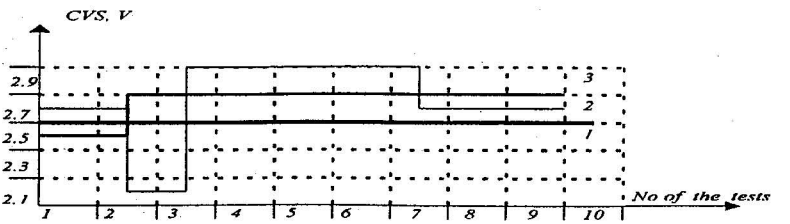

Fig.3. Measured CVS vs. number of the test 1 -before thermocycling, 2- after thermocycling, 3 - after 250,h temperature-controlled process

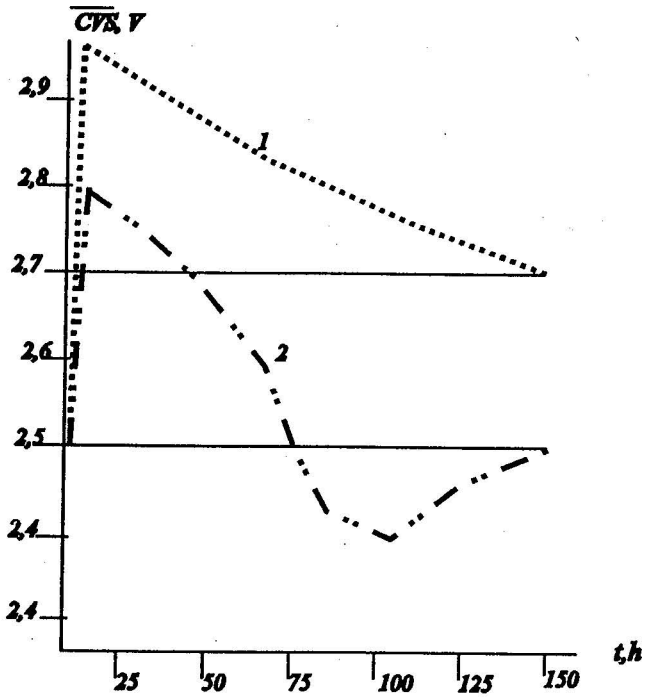

Fig.4. Measured $\overline{VCS}$ vs. time for batches 1 and 2

Measured variations of circuit's suitability criteria's limits are reversible and irreversible. These tests allow doing individual heat-resistance verification of IC during the incoming control. Fault localisation and further using of physical methods includes detecting of abnormal high critical voltage supply.

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