CAD in Electronics and Microelectronics Education

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Some ideas about the implementation of computer-aided design methods in the Electronics and Microelectronics engineering education are described in this article. Modern Electronics systems are characterised by their extreme complexity and sophistication, in which thousands and millions of components varying in operation and physical effects are integrated. Hence their understanding, studying and application is unthinkable without computer simulation, modelling, analysing and design.

The purpose of this paper is consideration of the possibilities for implementation of CAD systems with different complexity at different stages of the education and the presenting the experience of the ECAD Laboratory at the Faculty of Electronic Technologies, The Technical University of Sofia.

The basic approach in the application of CAD systems is the transition from simple to more complex design systems, so called top-down design, taking into consideration the already achieved knowledge by the students. Computer methods for simulation and design are used in special engineering subjects, course works, final year projects, etc.

The following software is applied in the education of students in Electronics engineering:

- Analysis and Synthesis of Analog and Digital-Analog Circuits - PSPICE, Design Centre;
- PCB Design - OrCAD, CADSTAR, EASY-PC;
- Top-down design of integrated circuits - CADENCE;
- System design applying VHDL - SYNOPSYS;
- ASIC design and prototyping - ALTERA, XILINX;
- Technological and physical simulation and design - PROMIS, MINIMOS, ZOMBIE, BAMBI, BIPOLE, etc.;

As a conclusion it should be emphasised that the participation of the Technical University - Sofia in EUROPRACTICE initiative is rather useful for the acquisition of software products, their upgrade and service.

INTRODUCTION

The contemporary development of Electronics is characterised by constant increasing of the IC level of integration and decreasing the device's geometry. Various numbers of physical principals of functioning and behavioural functions are being integrated together with the integration of enormous number of elements in a single chip. The advance in integral circuits and system engineering is a great one, where new function and methodology principals are being employed The integration at functional (behavioural), device level and physical principals have to be considered at the Microelectronics processes and technologies level as well.

The understanding and studying of complex 2-D and 3-D physical processes of sub-micron device functioning and implementation principles of state-of the-art technologies require the utilisation of complex software products which on their part suggest the availability of enormous computer resources. This is also applied to a greater extent to the methods of functional, logical, circuit and layout design, test vectors synthesis, and verification of the design.

The purpose of this paper is consideration of the possibilities for implementation of CAD systems with different complexity at different stages of the education and the presenting the experience of the Electronics Computer Aided Design Laboratory at the Faculty of Electronic Technologies, The Technical University of Sofia.

CAD IN DIFFERENT STAGES OF ENGINEERING EDUCATION

The Computer Aided Design is implemented in different rate, ways, depth and depending on the extent of engineering education in Electronics and Microelectronics. We shall discuss here only some of the practical questions without referring to the details of the methodology and pedagogic aspects in education.

In the early years of education, after studying the general subjects, treating the principles of design, functioning and utilisation of computers and fundamental programming languages a number of simple Microelectronics structure, device and technological processes simulation and design software products were implemented. Some of them are listed below: BIPOLE, MINIMOS, ZOMBIE, BAMBI, PROMIS, etc. The purpose is to make the students acquainted with the main function principles of the basic electronic devices, the influence of different semiconductor's technology parameters and alteration of external conditions upon 2-D and 3-D physical effects of semiconductor devices. The main electrical, physical and exploitation parameters and characteristics are studied. When

studying Microelectronics technologies the bipolar and CMOS fabrication processes are simulated. During that stage sample technological schemes are designed for creation of semiconductor structures with specific properties

The next stage in the education is the utilisation of standard professional CAD systems. In the beginning separate modules are being studied and implemented in the introduction to the theory of electrical end electronic circuits. Thus for example the Design Centre software package has a significant application in the teaching of the subjects Theory of Electric Circuits, Theory of Electronic Circuits, Analog Circuits, etc. After getting acquainted with the common structure of the software package students study in details the analog simulation module, models of electronic devices and optimisation methods. After that students study the digital, digital-analog simulation, filter synthesis, etc.

At the same stage of education students get acquainted with the professional design software packages for PCB design OrCAD, EASY-PC and CADSTAR. The special features of element placement, package types, routing, parasitics are being discussed here. Special attention is paid to the final documentation of course projects.

In recent years of education diploma projects are accomplished with the implementation of the software packages CADENCE and SYNOPSYS. When utilising the top-down design method one have to go through all main step for the design of a silicon chip. Students are encouraged to take part in real projects, including industry contracts. Different design approaches of an electronic system are possible. After the synthesis of structural schematic with the help of SYNOPSYS it is possible to transfer the design into silicon by the means of CADENCE, or by programming an FPGA circuit with ALTERA or XILINX.

HARDWARE ORGANISATION AT THE ELECTRONICS COMPUTER AIDED DESIGN LABORATORY

The Electronics Computer Aided Design Laboratory (ECAD) which is situated in Building No. 1 of the Technical University is equipped with hardware and software in the framework of the TEMPUS JEP 03038 - fig 1.

The hardware comprises IBM PC compatible computers - 486 DX2 / 66 MHz and PENTIUMs, and four SUN SPARCstations. Laser jet and matrix printers, as well as a pen plotter, a scanner and a modem are also available in the Laboratory. One of the workstations and two of the Personal Computers are situated in Building No 2 of the Technical University.

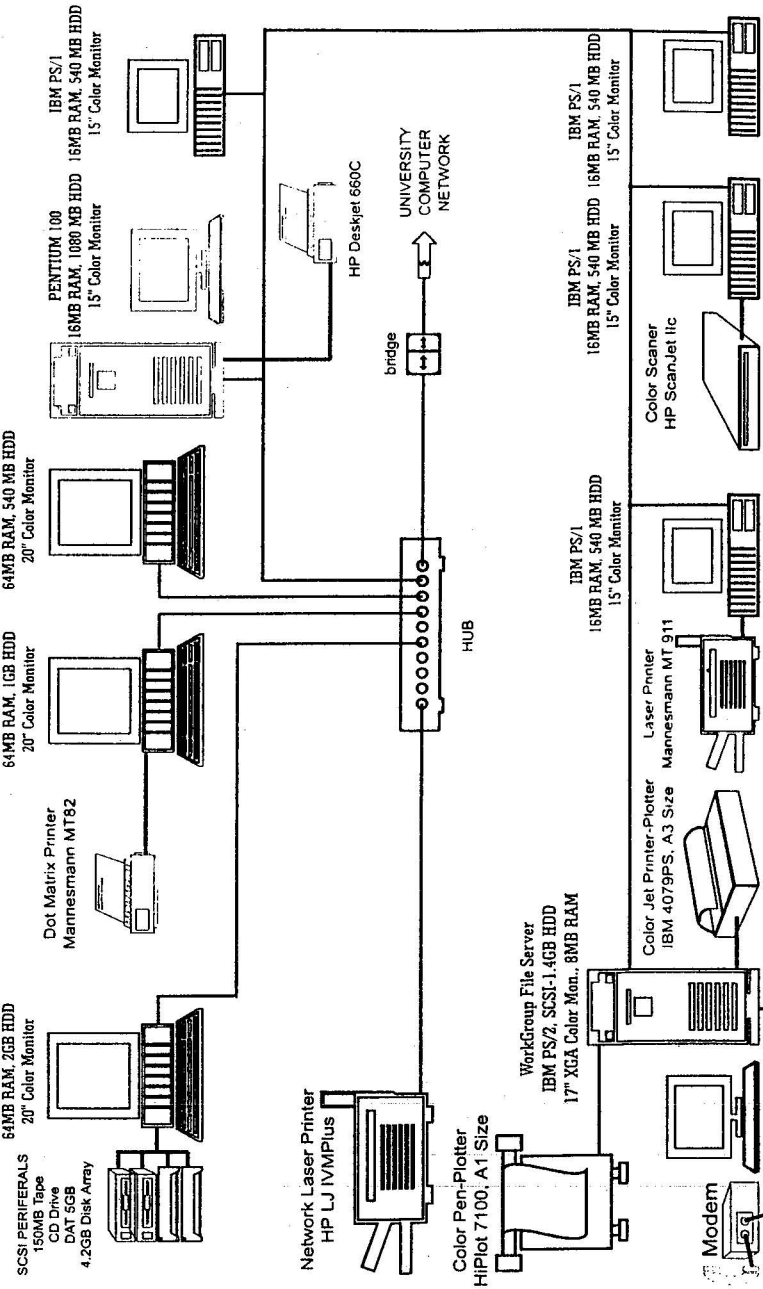

SUN SparcStation 10
64MB RAM, 2GB HDD
20" Color Monitor
SCSI PERIFERALS
150MB Tape
CD Drive
DAT 5GB
4.2GB Disk Array
Dot Matrix Printer
Mannesmann MT82
SUN SparcStation 10
64MB RAM, 1GB HDD
20" Color Monitor
SUN SparcStation 4
64MB RAM, 540 MB HDD
20" Color Monitor
PENTIUM 100
16MB RAM, 1080 MB HDD
15" Color Monitor
IBM PS/1
16MB RAM, 540 MB HDD
15" Color Monitor
HP Deskjet 660C
bridge
UNIVERSITY
COMPUTER
NETWORK
HUB
Network Laser Printer
HP LJ IVMPlus
Color Pen-Plotter
HiPlot 7100, A1 Size
WorkGroup File Server
IBM PS/2, SCSI-1.4GB HDD
17" XGA Color Mon., 8MB RAM
Color Jet Printer-Plotter
IBM 4079PS, A3 Size
Laser Printer
Mannesmann MT 911
IBM PS/1
16MB RAM, 540 MB HDD
15" Color Monitor
IBM PS/1
16MB RAM, 540 MB HDD
15" Color Monitor
Color Scaner
HP ScanJet IIc
IBM PS/1
16MB RAM, 540 MB HDD
15" Color Monitor
Modem

Fig 1.

SOFTWARE FOR PROFESSIONAL AND EDUCATIONAL APPLICATION

CADENCE

Overview

Cadence Design Framework II is a common interface of the complete range of CADENCE IC design tools. Using a common database and user interface, the framework allows easy cross checking between the various stages of the design flow, e.g. comparing the layout and schematic. There are a lot of data translators from and to CAD systems of other manufacturers, which makes CADENCE an opened system and in that way CADENCE is easy to integrate in any ASIC automatic design environment - fig. 2.

CADENCE Design Framework II Design Kits that are used in the Laboratory are as follows:

- ES2 - 1.0 μm; 0.7 μm CMOS;
- MIETEC - 2 μm; 0.5 μm;
- MIETEC - HBIMOS;
- AMS - 1.2 μm; 0.7 μm;
- AMS - 1.2 μm; BiCMOS;

Database Management

DFWII features a data management scheme which allows many users to work on the same design data, without ever causing concurrency violation, and which allows the tracking on a design trough any modification.

In addition to the UNIX permissions in the data, there is also a system of CADENCE permissions to allow some users to be given 'managers' rights.

Design Capture

CADENCE has a full schematic capture system, incorporating all of the usual features. In addition to the normal schematic features, CADENCE supports the embedding of VERILOG and VHDL descriptions into schematic.

The use of HDL allows a much more comprehensive "top down" philosophy to be used. At the start of the project the chip can be characterised by an HDL and as parts of it are turned into a schematic, those can be used to replace VHDL.

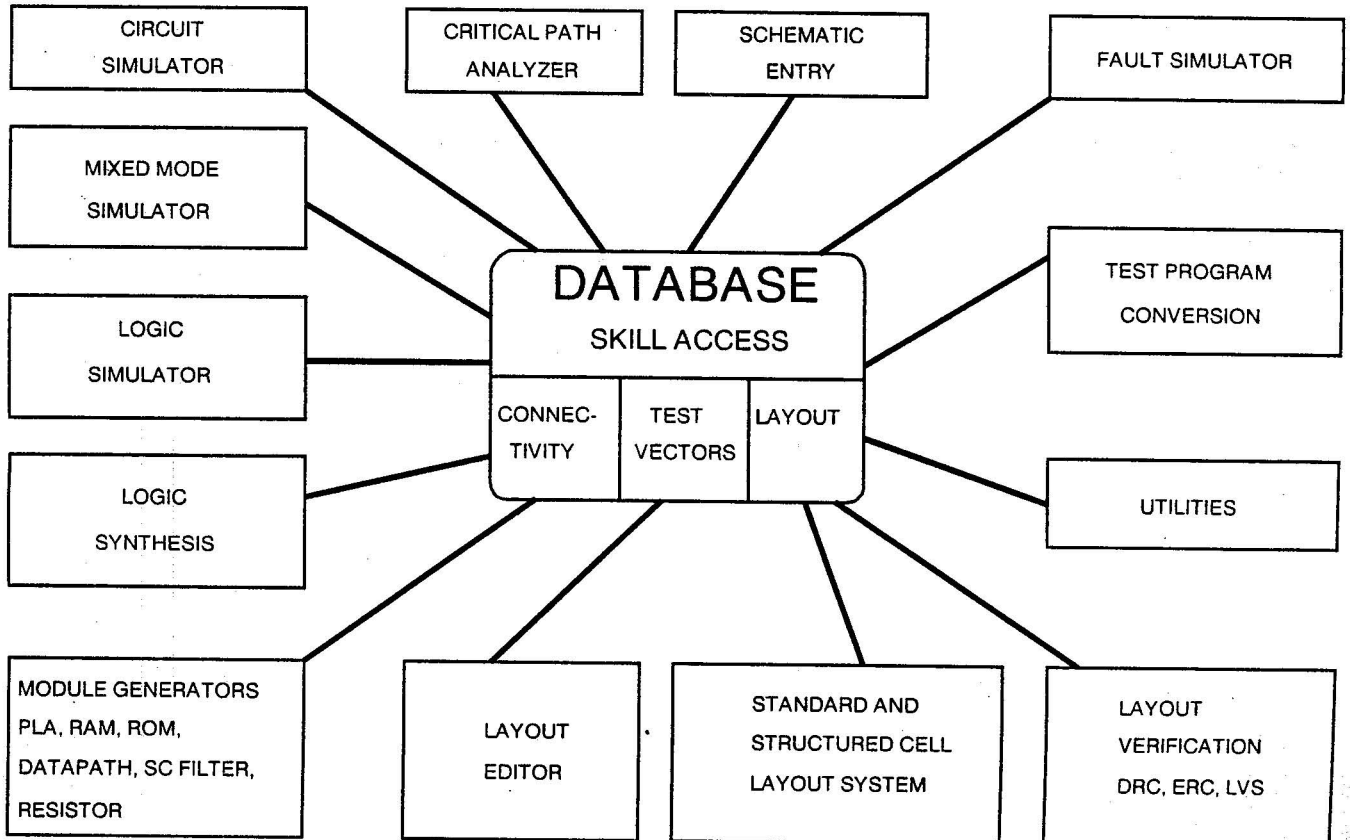

CIRCUIT SIMULATOR
CRITICAL PATH ANALYZER
SCHEMATIC ENTRY
FAULT SIMULATOR
MIXED MODE SIMULATOR
DATABASE
SKILL ACCESS
TEST PROGRAM CONVERSION
LOGIC SIMULATOR
CONNEC-TIVITY
TEST VECTORS
LAYOUT
LOGIC SYNTHESIS
UTILITIES
MODULE GENERATORS PLA, RAM, ROM, DATAPATH, SC FILTER, RESISTOR
LAYOUT EDITOR
STANDARD AND STRUCTURED CELL LAYOUT SYSTEM
LAYOUT VERIFICATION DRC, ERC, LVS

Fig. 2.

Simulation

In addition to using the HDL in design capture, provided you have certain information about your target library, you can simulate the HDL's in circuits which also contain schematic elements.

The simulation software also allows you to compare two simulation runs, so you can check that a schematic is the same as the HDL which it replaced.

Logic Synthesis

DFWII also features Synergy, a verilog based logic synthesis tool. From a verilog HDL description, Synergy can produce a gate level verilog description and a schematic.
The synthesis can be controlled to give output which is optimised for speed, or for minimum silicon area.

There is a possibility for integrating Synopsys as one of the most powerful synthesis systems fully based on VHDL.

Logic Simulation

CADENCE's Verilog-XL digital logic simulator is the core of the industry's most production-proven highest-performing top-down design environment.

Verilog-XL offers a single simulation environment for multiple levels of abstraction. Unlike other simulators, Verilog-XL fully supports mixed-level design, which one tool for architectural, behavioural, RTL gate and switch level design description.. And, it does so while reducing verification runtimes as a result of advanced algorithms and innovative simulation technique.

Mixed-Signal Simulation

CADENCE's Mixed-Signal Simulation Environment includes two leading simulators, Verilog-XL and a lot of advanced analog circuit simulators. like Spectre, cdsSpice etc. The Mixed-Signal Simulation Environment provides:

- Unique mixed-signal design environment to speed the design, simulation and analysis of high-performance mixed-signal circuits.
- Interactive simulation of mixed-signal design at multiple levels: behavioural, gate, switch, macromodel and circuit.
- Simulation of critical portions of the desired level of details.

Taking Design Into Silicon

Once the design has been entered and simulated, it must be turned into silicon. The most common way to do this is using automatic place and route. Each of the standard cells within the target library which you have been using will have been designed in silicon to make it easy to join to other cells in a row format. These rows of standard cells can be combined with custom layout blocks, or regular structures like ROMs and RAMs, and routed together

For more low level design, you can use a transistor level schematic, and convert t into layout synthesis tool LAS..

Cell Ensemble is a complete floorplanning and place and route system for cell-based integrated circuits. With a track record of thousands of production IC designs, Cell Ensemble has consistently met aggressive die size and performance goals at top semiconductor companies.

Post Layout Verification

In addition to the physical design verification necessary to ensure that the layout of the chip can be fabricated; it is also possible to simulate the complete chip using the actual data for interconnect delays, giving a truer picture of the chip final performance. This data can be compared to previous simulations to check that its function remains the same.

Virtuoso provides a hierarchical integrated circuit layout and verification environment that supports all IC design techniques, from hand crafting, to automatic component generation, compaction and layout synthesis.

Design Testability and Testing the chip

The synthesiser runs in concert with Synergy logic synthesis, so designers can simultaneously optimise their design for performance and testability.

The simulation data that was gained from the final simulation of the chip can be used to feed automatic test equipment with test vectors and expected outputs to ensure that the final silicon matches the design.

SYNOPSYS

Fig. 3 shows the skills that a designer must have to use SYNOPSYS.

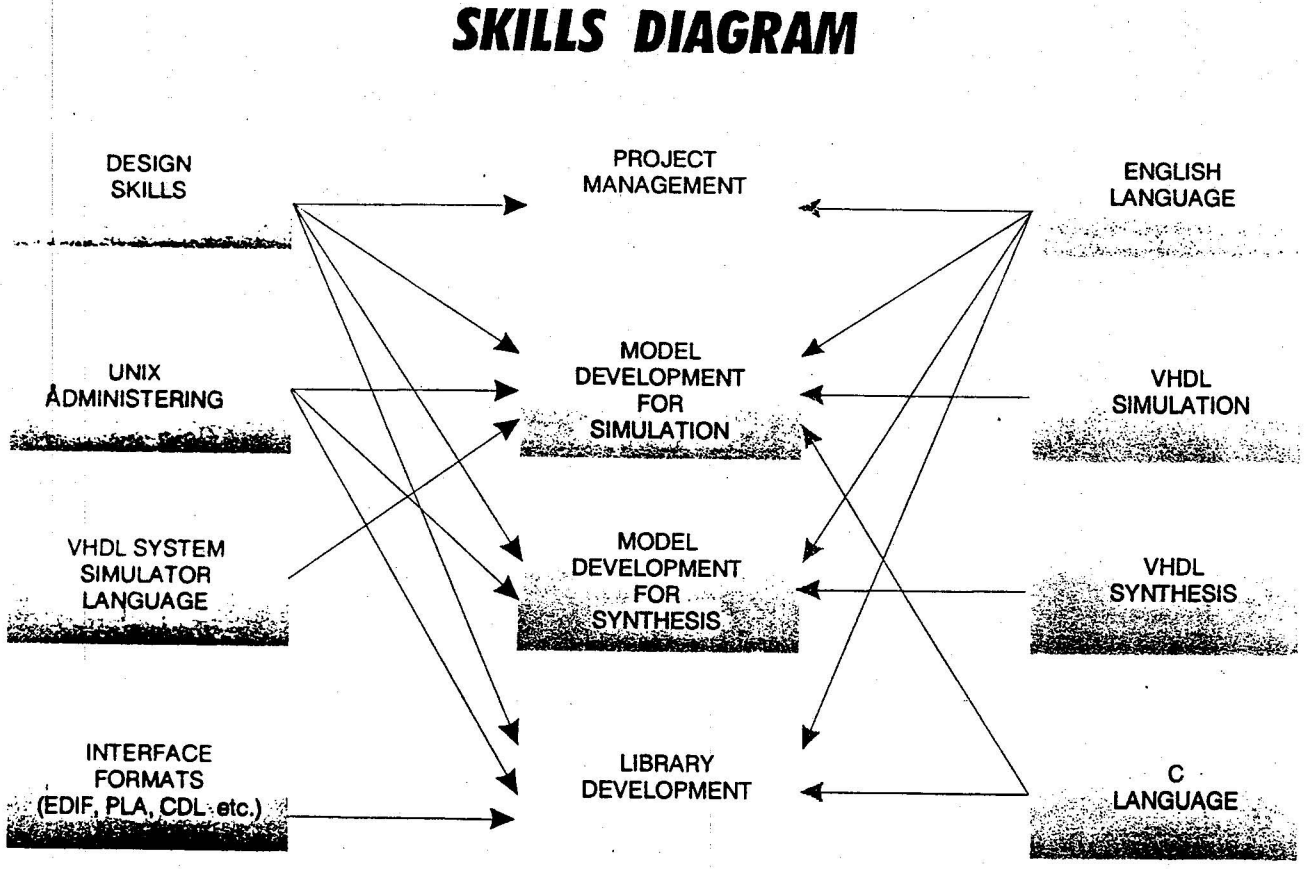

SKILLS DIAGRAM
DESIGN SKILLS
UNIX ADMINISTERING
VHDL SYSTEM SIMULATOR LANGUAGE
INTERFACE FORMATS (EDIF, PLA, CDL etc.)
PROJECT MANAGEMENT
MODEL DEVELOPMENT FOR SIMULATION
MODEL DEVELOPMENT FOR SYNTHESIS
LIBRARY DEVELOPMENT
ENGLISH LANGUAGE
VHDL SIMULATION
VHDL SYNTHESIS
C LANGUAGE

Fig. 3.

Fig. 4 shows the main steps for design using SYNOPSYS.

- ***Design Entry*** - input of initial information for the design using the interactive hardware description module (VHDL or Verilog);
- ***Validation*** of the initial data from the previous step - functionality and meeting the requirements.
- ***Implementation*** - different modules for logical and test synthesis in order to translate the netlist into specific technology.
- ***Verification*** of the synthesised circuit at a gate level. Development of HDL Testbench and test vectors.

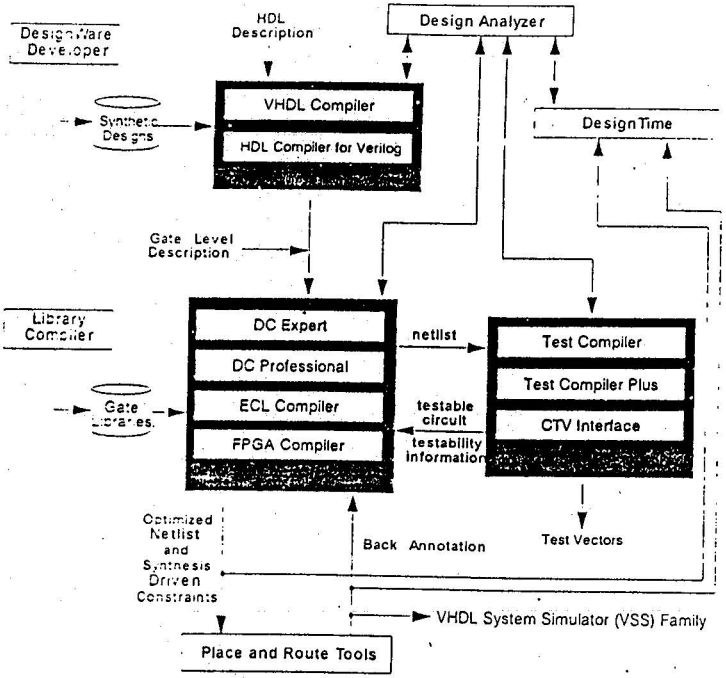
The SYNOPSYS application for digital circuit simulation includes:

- **Synopsys Graphical Environment**
  - ♦ **Schematic Editor**
  - ♦ **Symbol Editor**
  - ♦ **Hierarchy Navigator**
  - ♦ **VHDL Netlister**
- **Synopsys VSS (VHDL System Simulator)Family**
  - ♦ **VSS Expert**
  - ♦ **VSS Professional**
  - ♦ **VHDL Analyser**
  - ♦ **VHDL Simulator**
  - ♦ **VHDL Debugger**
  - ♦ **Waveform Viewer**
  - ♦ **Library Analyser**

Synopsys application for digital circuit synthesis

The synthesis applications are shown in fig. 5.
The Design Compiler family consists of four products:

- **DC Expert** - the most powerful tool for digital synthesis;
- **DC Professional** - set of tools for IC design;
- **FPGA Compiler** - design and optimisation of large set of programmable logical circuits.
- **ECL Compiler** - design of ECL circuits.



Logic Synthesis

The transfer from an HDL, such as Verilog or VHDL, to gate level is shown below:

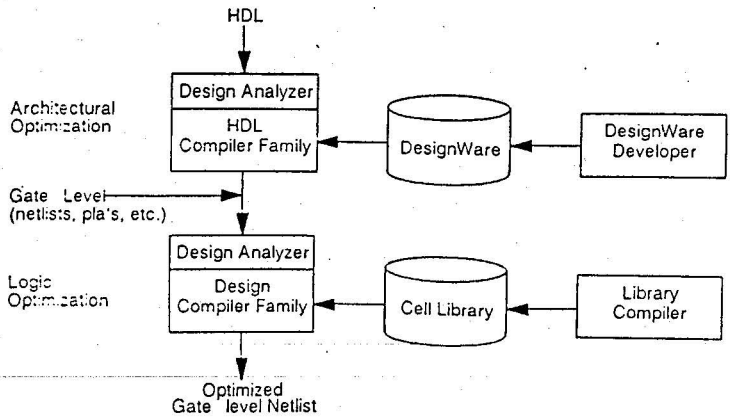


Fig. 4.

Synopsys Products

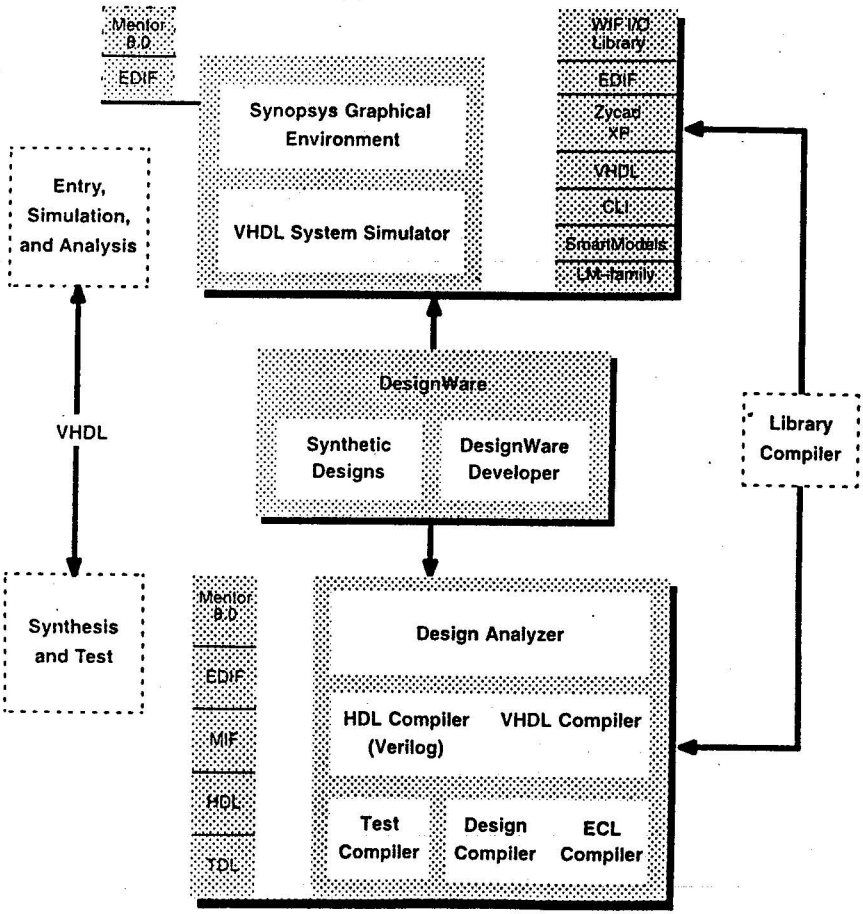


Fig. 5.

THE DESIGN CENTRE

MicroSim's Design Center EDA system provides an integrated environment to capture, simulate, and analyse analog and digital circuit designs. The Design Centre is a "universal" circuit design environment, meaning that a wide variety of circuits can be defined and analysed ranging from precision instrumentation amplifiers, to switching power supplies, to digital control circuits, to passive filters. The Design Centre achieves this by integrating the capabilities of several programs:

- ***Schematics*** - the graphical circuit design environment allowing to create, edit, and print schematic drawings, as well as create new symbols, configure library files, create PSpice netlists for simulation, package schematic for use with an external layout editor, and create layout netlists.
- ***PSpice*** - the analog, digital, and mixed analog\digital simulator.
- ***Probe*** - the graphical waveform analyser used to view and manipulate PSpice simulation results.
- ***Stimulus Editor*** - the analog and digital stimulus generation tools.
- ***Parts*** - the utility for creating semiconductor device model and subcircuit definitions by estimating semiconductor model parameters.
- ***Filter Designer*** - the active and passive filter synthesis design aid.
- ***Polaris*** - signal integrity analysis.

The programs and features available to user will depend upon purchased particular computing platform and package. Each program can be run stand-alone. However, the beauty of the Design Centre is its ability to integrate these programs into a unified circuit design environment.

The highly integrated Design Centre configuration begins with Schematics. With Schematics, circuit drawings are interactively created using part symbols to represent devices and wire symbols for connectivity. In addition to graphically creating circuit design with Schematics, user can set up simulation parameters, run PSpice, and run Probe directly from the Schematics program. Circuit files are produced automatically from the circuit drawing and simulation specification entered by the user through Schematics' windowed interface. The process of creating the circuit files is transparent to the user. The Stimulus Editor, Parts, and the Filter Designer program are available as utility programs. The Polaris program is used to extract parasitics from a board layout (derived from Schematics circuit drawing), using an external PCB layout package. Polaris is run directly from the Schematics program, producing a netlist that can be directly simulated using PSpice.

The following analyses can be set up in the Schematics before a simulation is initiated:

*** Standard**

- *AC Sweep* - Frequency response is calculated with one or more sources sweep over a range of frequencies.
- *Bias Point* - Additional bias point data is calculated and reported.
- *DC Sweep* - Voltages, currents, and digital states of the circuit's steady-state response are calculated with a source, model parameter, global parameter, or temperature swept over a range.
- *Transient* - Circuit behaviour is tracked over time in response to time-varying sources. The voltages, currents, and digital states are computed. For digital devices, the propagation delays can be set to minimum, typical, and maximum. If digital worst-case timing is selected, then PSpice simulation considers all possible combinations of propagation delays within the minimum and maximum range for digital devices.
- *Small-Signal Transfer* - Small-signal gain, input resistance, and output resistance is calculated as a function of bias point.

*** Simple Multi-Run**

- *Parametric* - Repeats standard analyses as a model parameter, component value, global parameter, or temperature is stepped through a series of values.
- *Temperature* - Repeats standard analyses as the temperature is stepped through a series of values.

*** Statistical**

- *Monte Carlo* - Iteratively computes circuit response to changes in component value by randomly varying all device model parameters which have tolerances specified for them.
- *Sensitivity\Worst-Case* - Computes circuit response to changes in component value by varying one device model parameter (tolerance specified) at a time on a device basis, culminating in a single run where all model parameters for all devices are set to their worst-case values.

Schematics - comes complete with support for hierarchical designs with multiple views, integrated symbols and package editing, symbol and package libraries

containing over 13 000 analog and digital parts, and interfaces to CADStar, PADS, P-CAD, Protel, SCICARDS, and TangoPRO board layout packages. Schematics also provides an EDIF netlist interface to board layout.

PSpice A/D - Mixed analog/digital simulation offers the full range of features available in both PSpice and PLogic. The analog and logic simulation algorithms are tightly coupled within the same program. The simulator automatically recognised and processes the A-to-D and D-to-A interfaces in your circuit. Simulation results are displayed together along a common time axis.

PSpice - Analog simulation capabilities provide a variety of standard analyses, as well as statistical analyses, analog behavioural modelling, graphical waveform analysis, performance analysis of simulation results, graphical stimulus editing, semi-automatic semiconductor device characterisation from manufactures' data sheets, and analog model libraries containing over 7 000 discrete devices.

PLogic - Digital simulation using event-driven logic processing techniques with 5 logic levels and 64 output strengths, digital worst-case timing analysis, warning message generation for timing violations and worst-case timing hazards, device modelling from databook specifications using logic expressions, pin-to-pin delay specifications, timing constraints and low-level primitives, graphical waveform analysis, graphical stimulus editing, and digital libraries for 17 different logic families totalling over 1 800 components.

PLSyn - Programmable logic synthesis combines device-independent, mixed-level design capture, efficient min-max timing simulation, optimised logic synthesis, and automated goal-and-constraint directed device selection. An automatic logic partitioning algorithm is available which can split the design into several parts to accomplish the physical design goals or implement large design. Choose from three Design Modules consisting of over 4 100 devices from 22 manufactures which include speed, price, power, packaging, and logic architecture information.

Polaris - Analysis tool for extracting transmission line, parasitic capacitance, and coupling values from printed circuit board layouts. Extracted values are then applied to circuit simulations using PSpice or PSpice A/D, providing fore analysis of crosstalk, reflection, and delay effects in the circuit design. The supported board layout formats include CADStar, PADS, P-CAD, and TangoPRO.

Mentor Integration - Custom interface to Mentor Graphics' environment (Falcon Framework) allows to simulate design entered in Mentor's Design Architect schematic editor using PSpice or PSpice A/D, and to conduct post

simulation analysis using graphical waveform analyser, Probe. Cross-probing is also supported.

Cadence Integration - Custom interface to Cadence Design Systems' environment (Design Framework II) allows to simulate design entered in Cadence's Composer editor using PSpice or PSpice A/D, and to conduct post simulation analysis using graphical waveform analyser, Probe. Cross-probing is also supported.

Device Equations - Partial source code for semiconductor devices only.

Filter Synthesis - Interactive design aid for the synthesis and analysis of active and passive filters, supporting RC active, switched-capacitor, and LC ladder filters; includes a menu-driven interface, hard copy report summaries and plots, concatenation of multiple designs, schematic displays of circuit topologies, and a netlist interface to PSpice A/D, PSpice, and SWITCAP.

CONCLUSIONS

- Optimal design and construction of hardware Utilisation of cheap PCs as terminals attached to the SUN workstations and complex and expensive educational software. Utilisation of comparatively slow remote computers for on-line work with complex packages;
- Visualisation and study of the top-down design method using the CADENCE uniform design system. Students not only utilise the standard features of the system, but they design and develop new modules, new standard cells, needed for their designs, discrete elements, new libraries (Design Kits) for other technologies, full-custom designed circuits;
- Utilisation of different software packages for the accomplishment of one and the same design step (for example Design Centre and CADENCE for analog simulation) In that way the identity of the models and physical objects that are used can be proven;
- Implementation of a connection (which is not supposed to appear in the products) between different big systems;
- Utilisation of cheap computers and software for fulfilment of some slow designs stages that require participation of many people. Utilisation of the achieved results in later stages in complex systems (effective utilisation of expensive hardware and software for education).
- Proper choice (for methodological and pedagogic purposes) of various simple, easy to use and cheap software packages in different stages of education for various purposes.

- Encourage students in their choice of proper software package for optimal decision of a particular problem.
- Student involvement in real engineering designs (team work, international teams, responsibilities, technical and economic analysis of the design, documentation, foreign language)

REFERENCES

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2. SYNOPSYS User Guide, Synopsys Inc., 1996
3. The Design Centre, MicroSim Corp., 1993