A PARALLEL RESISTORLESS CMOS ADC

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Abstract- A new type of parallel analog-to-digital converter (ADC) is proposed and investigated. The architecture of the converter is asynchronous, i.e. the comparators work without a clock signal. This approach avoids the noise involved by the clock signal feedthrough and reduces the power consumption in comparison with conventional synchronous flash ADCs. The main feature of the proposed ADC is the lack of a resistive voltage divider. The circuit design technique is based on the use of an originally developed CMOS comparator. Its entirely symmetrical circuit consists of an inverter input stage and two loops of a positive (PF) and a delayed negative (NF) feedbacks. The area ratio of the input CMOS transistors determines the threshold of the comparator instead of a reference resistor ladder. The interaction between PF and delayed NF yields a time-domain phenomenon called by the authors "dynamic hysteresis". As a result the comparator features one threshold, maximal switching rate and short-time noise immunity, determined by the NF delay. Simulations and experimental results proving the operation of the proposed ADC are reported.

I. Introduction. The most commonly used parallel analog-to-digital (AD) converters (ADCs) are based on the conventional synchronous "flash" architecture shown in Fig.1. The analog signal to be digitized is applied simultaneously to a bank of latched comparators. The reference voltage input for each comparator is derived from a resistive voltage divider. Under sampling clock, all comparators below the analog input level turn on, while those above it turn off. The resulting "thermometer code" is transformed into binary one by a code converter.The major flash ADC drawbacks are the high power consumption and noise involved by the clock signal feedthrough [1,2]. The proposed asynchronous architecture (Fig. 2) contains only comparators without any reference resistors or voltages, hence the comparator is the key element of the new ADC design.

II. Comparator circuit design. In Fig. 3 is depicted a model of the proposed comparator with internal reference voltage V_r. The positive feedback (PF) allows reaching maximal switching rate. Thanks to the PF inherent hysteresis, the comparator input is blocked just after the start of the switching process, for it is not susceptible to input noises. The hysteresis lasts till the arrival of the delayed negative feedback (NF) signal which cuts the PF loop and recovers the initial state of the circuit. This time-domain effect named by the authors "dynamic hysteresis" [5], ensures one threshold and short-time noise immunity, determined by the NF delay. Circuit design technique is based on a CMOS Schmitt trigger (Fig. 4) proposed in [3]. The developed topology shown in Fig. 5 is entirely symmetrical and in keeping with the features of the model. Firstly, the threshold of each ADC comparator could be obtained changing area ratio of the input transistors M1 and M2. Secondly, a chain of odd number inverters represents the PF delay. Thirdly, the PF and NF signals interact through transistor cascades M3,M4 or M5,M6.

III. Principle of operation. Let us suppose the input voltage level in Fig. 5 is below the threshold of the input inverter (M1,M2). The output voltage (inverter M7,M8) is low and transistor M4 is off. At the same time the NF output (M13,M14) is high, transistor M3 is on , allowing operation of the PF. When a raising signal reaches the input inverter threshold, the PF (inverter M6,M7 and transistor M4) begins switching. As a result the output signal of M1,M2 decreases, making the circuit insensible to fast changes, respectively noises, of the input signal. After arriving of the delayed NF signal, transistor M3 switches from on to off, interrupts the PF loop and restores the initial threshold. The opposite switching process caused by a decreasing input signal is the same, but the upper cascade M5,M6 is used for interaction of both feedbacks. *If the NF delay is controllable then the time domain insensibility should be adapted so that the noise added to the input signal to be rejected.* It is interesting to note that an asynchronous converter is rather a servo (tracking) ADC, i.e. at each conversion only one comparator is switching. Therefore, *the power consumption is distributed* over the whole signal period. Compared to a pure flash device, besides *switching noise reduction*, a substantial *power saving* is feasible.

IV. Simulations and experimental results. SPICE simulated input/output comparator waveforms (Fig. 6.a) depict expected one threshold behaviour. Because of the NF delay, at higher input frequency comparator can not react to fast signal changes and the predicted hysteresis is demonstrated, as shown in Fig. 6.b.

According to the proposed circuit design technique, a 3-bit ADC has been implemented by using 14007 chips. The input signal and output waveforms of two comparators are shown in Fig. 7. While the lower level comparator has only one threshold, the upper level comparator (narrower pulse) switches with hysteresis.

V. Conclusions. In this paper an asynchronous parallel resistorless ADC and corresponding comparator circuit have been proposed and investigated. The simulations, experimental and analytical results prove some advantages in terms of speed, noise immunity, power and area saving.

Appendix. Comparator threshold. The well known relation of transistor area ratio as a function of an inverter threshold V_{ri} , related to Fig. 8.a is :

$$\sqrt{\frac{\beta_P}{\beta_N}} = \frac{|V_{SS}| + V_{ri} - V_{TN}}{V_{DD} - V_{ri} - |V_{TP}|}$$

and is drawn in Fig. 8.b at $V_{DD}=IV_{SS}I=2.5V$, $V_{TN}=IV_{TP}I=1V$. In conventional AD and DA converters the components area ratio increases exponentially with the count of bits. Fig. 8.b shows that in the proposed ADC the maximal area ratio depends mainly on the input voltage range. For example a full scale range (FSR) of 1V (within -0.5V and +0.5V) needs maximal ratio of 4. In case of 2V FSR, this ratio is 25. Therefore a *substantial area saving* could be obtained especially at small FSR.

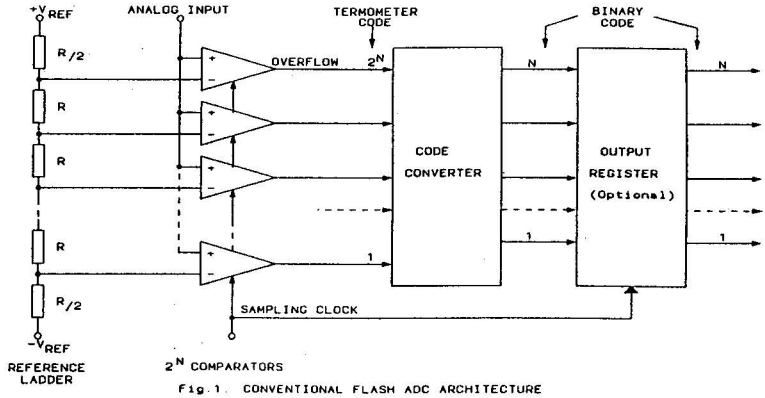


Fig.1. CONVENTIONAL FLASH ADC ARCHITECTURE

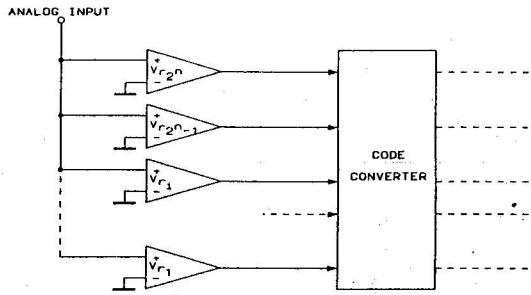


Fig.2. PROPOSED ASYNCHRONOUS ARCHITECTURE

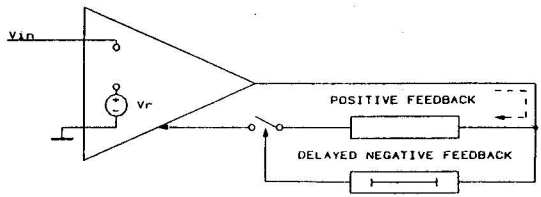


Fig 3 MODEL OF THE ASYNCHRONOUS COMPARATOR

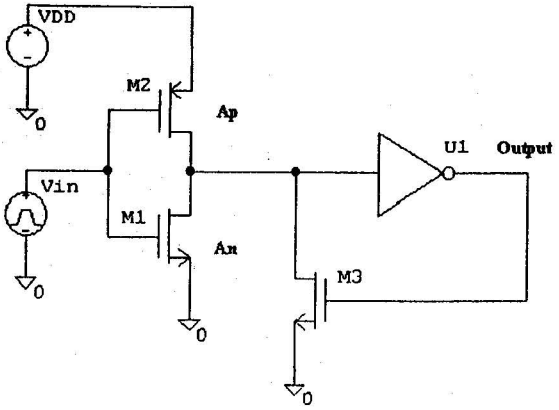


FIG.4. BASIC SCHMITT TRIGGER CIRCUIT

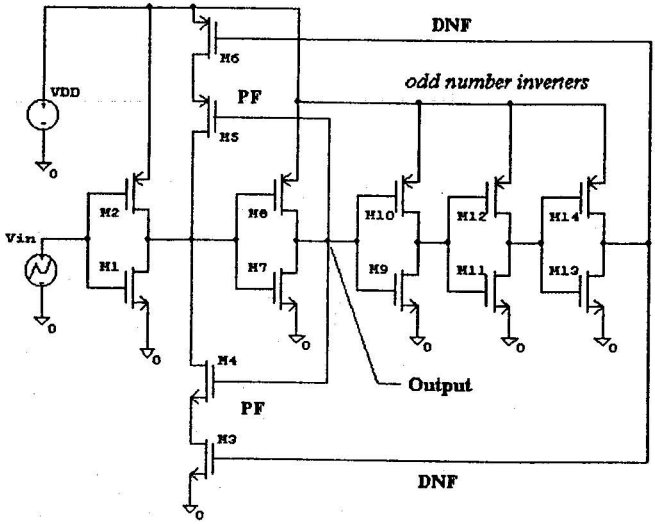
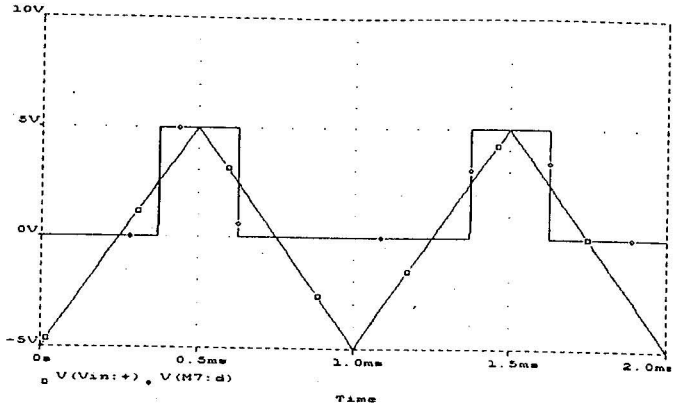
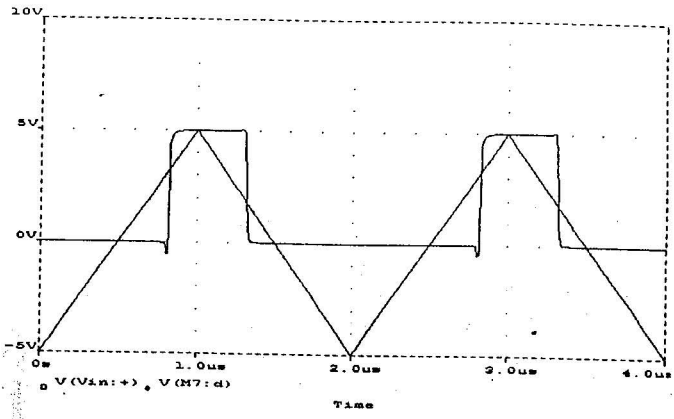


FIG.5. SCHEMATIC OF THE ASYNCHRONOUS COMPARATOR



a)



b)

FIG.6. SIMULATED BEHAVIOUR OF THE COMPARATOR AT a)LOW AND b)HIGH INPUT FREQUENCY

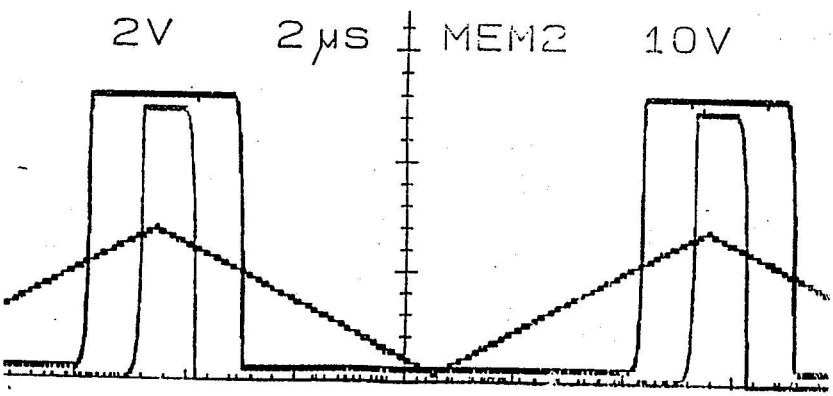
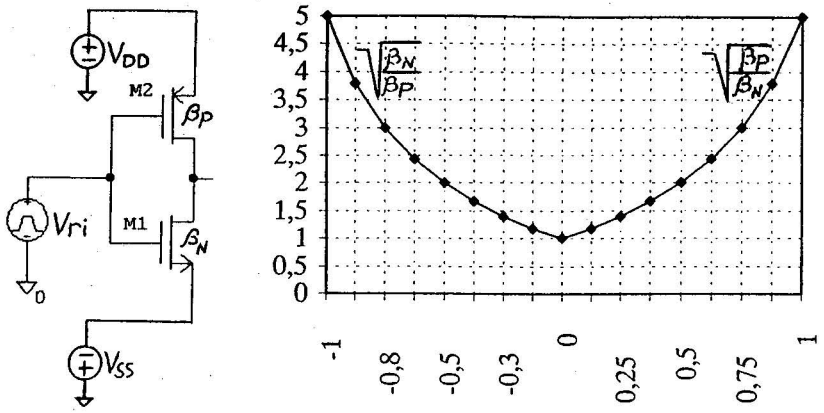


FIG.7. EXPERIMENTAL WAVEFORMS OF THE ANALOG INPUT AND TWO ADC COMPARATOR OUTPUTS



a) b)

Fig. 8. CMOS inverter (a) and transistor area ratio as a function of the inverter threshold V_{ri} (b).

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