Recent trends in translinear circuits

by

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I ***Summary***

This paper deals with recent developments in static and dynamic translinear (TL) circuits. First a review of the basic theory of traditional TL circuits is given, followed by some recent MOST TL circuits, where the back gate is employed as an extra signal terminal. Then, the recently found basic theory of dynamic TL circuits, together with an analysis/synthesis method is presented. Finally, a few examples at circuit-level will be given.

II *Introduction: static translinear circuits*

II-1 *Short historical review*

About the term "translinear"

Early translinear circuits were strictly based on the remarkable fact that the transconductance of a BJT is linearly proportional to its collector current. This fact is a consequence of the logarithmic relation between I_C and V_{BE}.

$$V_{BE} = V_T \ln\{I_C / I_S(T)\} \tag{1-1}$$

from which it follows

$$\frac{\delta I_C}{\delta V_{BE}} = g_m = \frac{I_C}{V_T} \tag{1-2}$$

This is the key to the strictly translinear principle and, basically, only devices showing a very exact logarithmic relation are suitable. As MOSTs operating in weak inversion show a comparable relation between the gate-source voltage and the drain current, they are suitable too for application of the strictly translinear principle.

A general property of a TL circuit is that it contains one or more closed loops of emitter-base junctions (gate-source junctions) with a voltage-current relation according to (1-1). However, over time the term "translinear" has come to refer to a wider class of circuits, for some "translinear" circuits contain MOSTs in strong inversion, whose Vgs-Id relation is quadratic instead of exponential, whereas the other properties (the presence of loops of gate-source junctions and/or the intentional use of the Vgs-Id relations) are maintained.

II-2 *General classification of translinear circuits within the world of analog circuits*

To begin with we consider a closed loop of junctions. We assume that all junctions (which can be diodes or the input ports of transistors) are forward-biased with external circuitry. Other boundary conditions are that the loop must contain an *even number of junctions (at least two)* and that there are *an equal number of junctions clockwise facing and counterclockwise facing* (shorted CW and CCW).

If the forward voltage of each junction (1, 2, 3, ...n) is V_{Fk}, it follows

$$\sum_{k=1}^{k=n} V_{Fk} = 0 \tag{1-3}$$

If we assume that V_T is device-independent and the collector current density (drain current per square) of any device is J, we easily derive [1]

$$\prod_{CW} J = \prod_{CCW} J \qquad (1\text{-}4)$$

Equation (1-4) gives the ultimate translinear principle, in words (Gilbert [1]):

In a closed loop containing an even number of forward biased junctions, arranged so that there are an equal number of clockwise facing and counterclockwise facing polarities, the product of the current densities in the clockwise direction is equal to the product of the current densities in the counterclockwise direction.

(For MOSTs in weak inversion the words "current densities" have to be replaced by "drain currents per square").

A special class of analog electronics that has attracted much interest during the last few decades is the design of *low-power/low-voltage* circuits. In this class we observe a revival of some types of translinear circuits. This is mainly because the *current-mode* operation of translinear circuits perfectly fits with *low-voltage* operation, whereas *low-power* operation generally implies that the system bandwidth is restricted. (Note, that the low-frequency area is the most powerful operation area of TL circuits). For all traditional (static) TL-circuits we refer to literature [2]

II-3 ***Suitable semiconductor components***

If we only consider circuits operating according to the *strict* translinear principle (Eq. 1-4), we must resort to devices with a perfectly exponential transfer. BJTs fulfill this requirement within a very large collector current range. Other suitable devices for the strictly translinear principle are MOSTs operating in weak inversion. If the *strictly* translinear principle is no longer maintained, MOSTs operating in moderate/strong inversion are also suitable.

III ***Analysis and synthesis methods for static translinear circuits***

III-1 ***Analysis***

The currents that play a role in any true static translinear circuit are the collector (drain) currents of the transistors, the biasing currents and the in-and output signal currents, Hence, analysis of TL circuits comes down to a description of all independent KCLs and all loop equations according to (1-4) followed by elimination of the undesired variables.

III-2 ***Synthesis of static TL circuits; the heuristic approach versus the systematic approach.***

III-2-1 ***The heuristic approach***

The term "heuristics" literally means "method of solving problems by inductive reasoning, by evaluating past experience and moving by trial and error to a solution". The first design approaches of most known electronic circuits were done in this way and, consequently, generally only experienced engineers are able to find new solutions by using this approach.

III-2-2 ***The systematic approach***

A systematic design system must contain a set of generally valuable, structured design rules. These rules must be structured in a hierarchical way, so that, from a restricted set of suitable basic configurations, all possible solutions to a preliminarily stated problem are generated. The approach has successfully been applied to the design of amplifiers with overall feedback and also to translinear circuits. The advantages of this approach are

twofold. First, a well-structured design system can be used by designers without specialized talent or experience. Second, it generally generates more (and sometimes better) solutions to the same problem than would have been found by heuristic designing. However, systematic design systems have some serious drawbacks too. Generally, the solutions generated by such systems preferably must be selected by an experienced designer, first because not all solutions are practically appreciable and second because some solutions don't work at all. The last phenomenon is because the system generally is not able to process *all* electrical properties. As an example: in synthesis systems for translinear circuits some resulting circuits may show positive feedback loops (possibly resulting in oscillation or latching) because the system is not able to recognize this item.

III-3 ***Interaction between the heuristic and the systematic approaches***

The development of systematic design systems has always been the result or continuation of much work carried out in a heuristic way. They are valuable to generalize and complete the heuristically found solutions. Therefore, the importance of heuristic reasoning should never be depreciated. However, new, systematically found solutions can deliver new impulse and fresh understanding to the heuristically reasoning designer. Almost all traditional static TL circuits have been heuristically found. Examples are *current mirrors, analog multipliers/dividers geometric mean circuits, "minimax" circuits, rms-dc converters,* and various circuits for (other) nonlinear signal processing [2]. Examples of systematically found static TL circuits can be found in [3].

III-4 ***Systematic synthesis methods for static TL circuits***

II-4-1 ***Introduction***

Because TL-circuits show common topological properties, they invite a systematic synthesis approach. Seevinck [4] has carried out extensive research into the analysis and synthesis of TL circuits with bipolar transistors of the same polarity. The synthesis method is restricted to TL-structures with < 10 branches and one or two loops. Thus, all possible topologies of TL-circuits with the restrictions mentioned and with a number of prescribed transfer functions can be synthesized. However, it is surprising that nearly all fruitful and promising topologies found, have earlier been found with heuristical methods. But this is not true in *all* cases.

As the methods are mainly based on network-theoretical and mathematical grounds, an extensive treatment lies beyond the scope of this book. Therefore we confine ourselves to a brief outline in Section IV-2 and refer to literature for details [4]. Further, an example of a useful TL-circuit obtained by synthesis, that was not found earlier, will be shown (See Section VIII).

III-4-2 ***The Seevinck synthesis method for bipolar semiconductor devices.***

The general aim is the design of static TL networks realizing a prescribed (non)linear, time-invariant transfer function. The strategy shows some similarity with traditional synthesis methods for passive networks. The synthesis procedure can be divided into four general steps:

1. Approximation of the prescribed function by suitable algebraic formulations
2. Decomposition of the algebraic formulations found into fosuitable for TL realization
3. Realization of networks, based on topological properties of those TL networks, which fit with the forms found in 2).

4. Selection of the networks found as to their complexity, cost, stability, sensitivity to parameter tolerances, etc.

The parts 1. through 3. will briefly be explained now.

1. ***Function approximation***

Only ***algebraic*** functions are suitable, of which ***rational*** functions need special attention, because they provide greater precision than polynomials of the same degree. Hence, non-algebraic functions need to be approximated by algebraic functions. As an example, a pretty accurate approximation of a sine function is given below

$$\sin \pi X \cong \frac{x - x^3}{1 + x^2}, \; for | X | \leq 1 \tag{2-1}$$

2. ***Function decomposition***

For synthesis purposes it is convenient to write the TL relation (1-4) in a slightly different form. Say that a TL loop has N elements (branches), numbered from 1 to N with branch currents I_1 through I_N, divided into odd and even ones, and with device areas A_1 through A_N, then (1-4) can be written as

$$\prod_{n=1}^{N/2} I_{2n} = \lambda \prod_{n=1}^{N/2} I_{2n-1} \;\text{ where }\; \lambda = \prod_{n=1}^{N/2} \frac{A_{2n}}{A_{2n-1}} \tag{2-2}$$

Any TL network has one or more input currents $I_{i1,2,...}$ and output currents $I_{o1,2...}$ Further, every branch current I_1 through I_N can be expressed in linear combinations of the input and output currents.

Generally, if the expressions of the branch currents into the input and output currents are called f_1 through f_N, application of (2-2) yields

$$f_1(I_{i1,2...} I_{o1,2...}) f_3(I_{i1,2...} I_{o1,2...}) \ldots = \lambda f_2(I_{i1,2...} I_{o1,2...}) f_3(I_{i1,2...} I_{o1,2...}) \ldots \tag{2-3}$$

Hence, function decomposition means that the prescribed function (approximation) is "translated" into forms according to (2-3).

Note: As all functions f_1 through f_N represent currents in TL elements, they must remain positive for all (positive and negative) values of the input and output currents. This must be checked after decomposition.

Many decomposition techniques are known in mathematics. Suitable techniques for TL synthesis are those using *explicit forms; implicit forms; parametric forms; rational functions; continual fractions,* etc. Generally, each of them is suitable for a class of function approximations. As an example we give the implicit decomposition of the sine function of (2-1)

$$\frac{1 + z + x}{1 - z - x} = \frac{(1 + x)^2}{(1 - x)^2} \tag{2-4}$$

where z is the output signal. For further details we resort to referring to literature [3].

3. ***Network realization techniques***

An arbitrary TL network always contains one or more (interwoven) TL loops with minimally four branches. If the branch currents and node voltages are left out of consideration and if, besides, every TL element is symbolized by a line, the result is the so-called *undirected graph* of the TL network. Every graph represents a class of TL networks. Of course, the number of branches (=TL elements) is theoretically unlimited.

However, due to practical parameter tolerances it has been shown to be senseless to construct TL networks with more than 9 branches and/or more than 2 loops. This limitation results in maximally 6 different graphs. Any graph can more precisely be characterized by numbering its nodes and choosing the direction of the branch currents. Then every graph has a corresponding ***node-branch incidence matrix (the T matrix).*** The total number of different T matrices corresponding to the 6 graphs amounts to 26. To date, the connections of the in- and output currents and the values and connections of biasing currents have not yet been chosen. Hence, it will be clear that any T matrix generally results in a great number of possible TL networks. Checking them all would be possible, but this immense job would be entirely a matter of *analysis*, and give hardly any insight. To make a real ***synthesis*** of TL circuits feasible, the possible ***general function structure of the relations between the branch currents*** that can be realized by any graph, has to be investigated.

Now the synthesis procedure is as follows. First, the (approximation of the) desired function is decomposed in one or more ways, so that the results fit with one (or more) of the general function structures according to a suitable graph. Second, all possible T matrices are derived from the (directed) graphs. Third, all possible TL networks are derived from the T matrices. Finally, the resulting networks are checked and selected on feasibility and quality. It will be clear that with all 26 T matrices the realization of numerous different TL networks providing many (approximated) transfers is feasible [3].

IV ***Recent TL circuits with MOSTs (weak inversion) with back gate control***

A simple model for the drain current of a MOST in saturation and in weak inversion as a function of the gate-source and bulk-source voltages (V_{GS} and V_{BS}) is

$$I_{DS} = I_0 e^{V_{GS}/\kappa U_T} e^{(1-1/\kappa)V_{BS}/U_T} \qquad (4\text{-}1)$$

where $U_T = kT/q$ is the thermal voltage and κ is the subthreshold slope. An interesting property is gained, if V_{GS} and V_{BS} are driven with the same source signal V_S. From (4-1) it appears, that in that case the V_S/I_{DS} slope becomes $60mV$ / *decade* i.e. the same as with a bipolar transistor. A useful application is shown in Fig. 4-1b: the so-called *bulk current mirror* [6]. Here the forward- and back gate voltages are connected with a level shift, i.e. the source follower M_3 in Fig.4-1b.

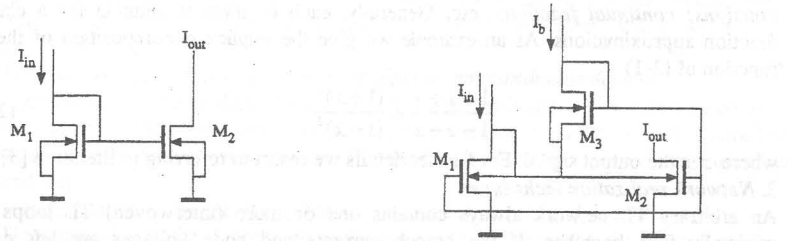


Fig. 4-1a,b Conventional MOST current mirror (left) versus bulk current mirror (right)

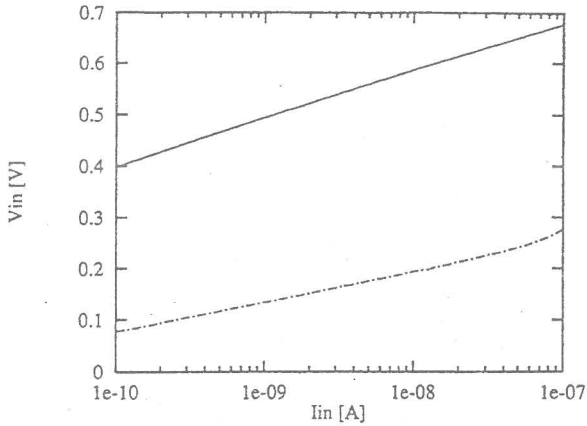
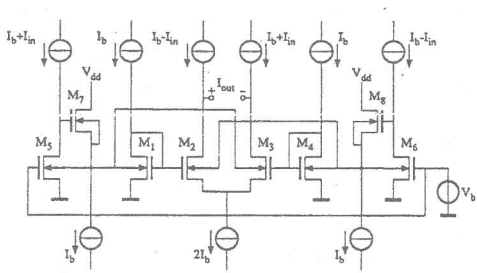


Fig.4-2 Measured input voltages of the conventional current mirror (solid) and the bulk mirror (dashed)

In Fig. 4-2 its measured input voltage as a function of its input current is compared with that of the conventional mirror, shown in Fig. 4-1a. Indeed, we observe a slope of $60mV$ / *decade*. Another application of the back gate is gained if, apart from gate-source loops, the bulk-source junctions are employed in separate TL loops. In other words, the MOSTs are used as true four terminal devices. If both types of loops are used in one TL circuit, it is feasible to realize more complicated functions with a given number of devices than with three terminal devices [6]. Fig. 4-3a depicts an example of such a structure, having two interwoven bulk-source loops and one gate-source loop.



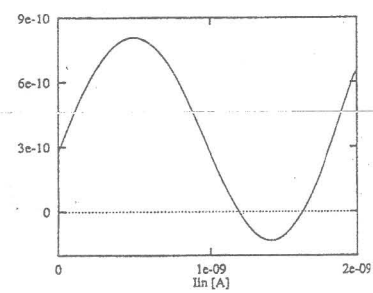


Fig. 4-3a, TL structure including bulk loops; Fig.4-3b, Measured output current.

Applying (4-1) and (1-4) for all loops, yields

$$\frac{I_1 I_3}{I_2 I_4} = \frac{I_5^2}{I_6^2} \tag{4-2}$$

This equation structure exactly fits with the decomposed sine function of (2-4). Hence, the loop structure in Fig. 4-3a is suitable for a TL realization of the sine function (2-4). Fig. 4-3b depicts the measured transfer.

A mayor drawback of back gate control is that the device becomes slow, so that its application is limited to low frequencies.

V Dynamic translinear circuits

V-1 Introduction

A brandnew field in the area of the translinear circuits are the *dynamic translinear circuits*. There is a growing interest in such circuits implying linear filters, oscillators, PLLs, etc. owing to a few special general properties. If we confine ourselves to filter circuits these properties are

- They are inherenly *instantaneously signal companding*, so that larger dynamic ranges can be realized (with given supply voltage and capacitor values) than with traditional filters without the addition of intermodulation distortion. Distortion free *syllabic* companding is also possible with this type of filters [7].
- Their connections with the outside world, i.e. other electronic circuitry, are inherenly at *current level*. This property makes them very suitable for low-voltage electronics.

V-2 Basic principle

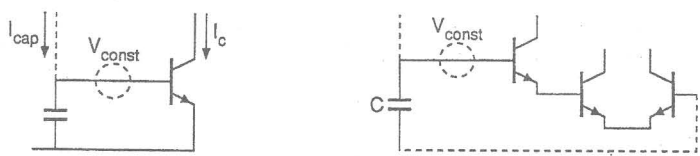


Fig. 5-1 a): Simplest loop including a capacitor; b): general case

The most simple partial circuit, and also the key of the principle of dynamic TL circuits, is shown in Fig. 5-1a, where the following relation yields

$$CU_T \frac{\partial I_C}{\partial_t} = I_C I_{cap} \tag{5-1}$$

Note that the left hand side of these equation is part of a differential equation and the right hand part is part of a polynomial, only containing ***currents.*** The principle can be generalized according to Fig. 5-1b, where

$$I_{cap} = CU_T \sum_i \pm \frac{\partial I_C / \partial t\,(i)}{I_{C,i}} \tag{5-2}$$

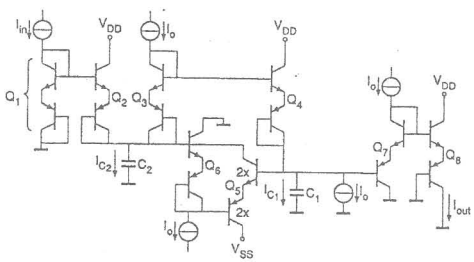
Due to the differentiation, V_{const} in Figs 5-1a,b may have an arbitrary value.

Hence, apart from traditional TL loops, containing an ***equal*** number of CW and CCW junctions, a dynamic TL circuit may also contain loops including a capacitor and an ***arbitrary*** number of CW and/or CCW junctions. Another difference between both types of loops is that traditional TL loops only contain collector currents, but that loops including capacitors also contain capacitor currents.

VI *Analysis of dynamic TL circuits*

Although a few examples of analysis methods are known from literature [4], the method presented here exclusively uses TL loop equations and consequently is very obvious and flexible. The method is represented schematically in Fig. 6 illustrated with an example: the analysis of a second order filter, known from literature, i.e. a second-order low-pass filter.

INPUT: detailed circuit diagram



Step 1

TL-loops: $Q_1 - Q_2 - Q_3 - Q_4 - Q_7 - Q_8 \Rightarrow$

$I_1 I_3 I_7 = I_2 I_4 I_6$

$Q_3 - Q_4 - Q_5 - Q_6 \Rightarrow$

$I_3 I_6 = \frac{1}{2} I_4 I_5$ (Q_5: double area)

KCLs at terminal C's: $I_2 + I_3 = I_{C2}$

$I_4 = I_{C1} + I_o$

Step 2

Substitution external currents:

$$\begin{cases} I_1 = I_{1n} \\ I_3 = I_o \\ I_6 = I_o \\ I_7 = I_o \\ I_8 = I_{out} \end{cases}$$

Resulting equations:

$$\left.\begin{array}{ll} ① & I_{1n} \quad I_o^2 = I_2(I_{C1} + I_o)I_{out} \\ ② & 2 \quad I_o^2 = (I_{C1} + I_o)(I_2 + I_4 - I_{C2}) \end{array}\right\} = \text{equations Set 1}$$

Transfer $\frac{I_{out}}{I_{in}}$ has 4 unknowns:

I_{out}, I_{C1}, I_{C2}, I_2

Step 3

Two loops containing the capacitor voltages

③ $C_1 - Q_7 - Q_8$:

$$I_{C1} = C_1(2U_T)\frac{\dot{I}_{out}}{I_{out}}$$

④ $C_2 - Q_3 - Q_4 - Q_7 - Q_8$:

$$I_{C2} = C_2(2U_T)\left(\frac{\dot{I}_{C1}}{I_{C1} + I_o} + \frac{\dot{I}_{out}}{I_{out}}\right)$$

$\Big\}$ = equations Set 2

Step 4

Substitutions:

- I_{C1} and $\dot{I}_{C1}$ (from ③) substituted into ④

  Result: explicit expression for I_{C2}

- Substitution of I_{C1} and I_{C2} into ① and ②

  Result: two equations with two unknowns: I_2 and I_{out}

- Elimination of I_2 yields

$$C_1C_2(2U_T)^2\ddot{I}_{out} + (C_2 - C_1)(2U_T)I_o\dot{I}_{out} + I_o^2 I_{out} = I_o^2 I_{1n}$$

Normalization:

Substitute $C_1' = \frac{2U_T C_1}{I_o}$ and $C_2' = \frac{2U_T C_2}{I_o} \Rightarrow$

$$C_1'C_2'\ddot{I}_{out} + (C_2' - C_1')\dot{I}_{out} + I_{out} = I_{1n}$$

Laplace:

$$\mathcal{L}\left\{\frac{I_{out}}{I_{1n}}\right\} = \frac{1}{s^2C_1'C_2' + s(C_2' - C_1') + 1}$$

Frequency transfer $s \rightarrow j\omega$; Butterworth if

$$\frac{I_{out}}{I_{1n}}(\omega) = -\frac{1}{\frac{\omega^2}{\omega_o^2} - j\frac{\omega}{\omega_o}\sqrt{2} - 1}$$

Fig. 6, Illustration of the analysis procedure for dynamic TL circuits

VII *Synthesis of dynamic TL circuits*

Starting with the dimension free differential equation (DE) of the desired electric behavior of the circuit to design, the DE is converted into one at current level and in the time domain, by suitable dimension transforms. Then the derivatives of the DE are replaced by parts of polynomials in the current domain, with the aid of equation structures like (5-1) and (5-2). The next step is decomposition of the resulting polynomial into suitable TL loop equations. A systematic method for steps 3 and 4 is not yet completed. Basically the decomposition method, discussed in Section 2 could also be used for decomposition of equations for ***dynamic*** TL circuits. However, due to the capacitor currents this is much more complicated than with equations for ***static*** TL circuits, so that a suitable decomposition is often hard to find. Research is going on, employing methods of the symbolic algebra and will be published in the foreseeable future. The final step is the construction of a TL version on transistor-level with the loop equations found. Fig. 7 depicts an example: With a dimension free DE of a second-order low-pass Butterworth transfer as the input, a circuit at transistor level of such a filter is derived.

INPUT: Dimensionless DE:

$$\ddot{z} + \sqrt{2}\,\dot{z} + z = x$$

output input

$\dot{z}$ and $\ddot{z}$: dimensionless "time" derivatives:

$$\dot{z} = \frac{\partial}{\partial \tau} \text{ and } \ddot{z} = \frac{\partial^2}{\partial \tau^2}$$

Step 1: Add Dimensions:

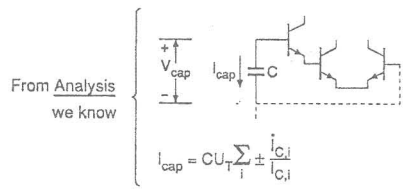
- current: $x = \frac{I_{in}}{I_o}$ $z = \frac{I_{out}}{I_o}$
- time: $\frac{\partial}{\partial \tau} = \frac{\sqrt{2}CU_T}{I_o} \frac{\partial}{\partial t}$ (dimension [s])

RESULT: Current-mode DE:

$$2C^2U_T^2\ddot{I}_{out} + 2CU_TI_o\dot{I}_{out} + I_o^2I_{out} = I_o^2I_{in}$$

Step 2: Definition capacitor currents:

From Analysis we know



$$I_{cap} = CU_T \sum_i \pm \frac{\dot{I}_{C,i}}{I_{C,i}}$$

2 capacitors needed

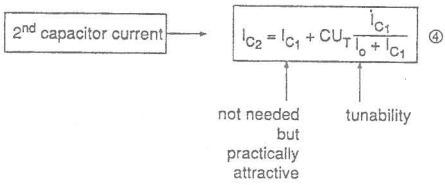
1st capacitor current → $I_{C1} = CU_T \frac{\dot{I}_{out}}{I_{out}}$ ①

$$\dot{I}_{out} = \frac{I_{out}I_{C1}}{CU_T}$$ ②

Substitution of ① and ② into the current mode DE reduces its order by one!

$$I_{out}(2CU_T\dot{I}_{C_1} + 2I_{C_1}^2 + 2I_{C_1}I_o + I_o^2 = I_{in}I_o^2$$ ③

Step 2: Continued



Substitution derivation of $\dot{I}_{C_1}$ from ④, and substitution into ③ yields

$$I_{out}(2I_{C_1}I_{C_2} + 2I_{C_2}I_o + I_o^2) = I_{in}I_o^2 \qquad ⑤$$

⑤ is the desired current-mode polynomial without derivatives

Step 3: TL-Decomposition

OBJECTIVE:

Conversion of the current-mode polynomial into TL-loop equations

Techniques: same as with static TL-circuits

but

→ more complex polynomials → more difficult

→ in nearly all cases more than one loop } ⇒ parametric decomposition necessary

→ subject of present research:

development of software using methods of symbolic algebra

In simple cases heuristic solutions possible

In the present example (2nd order Butterworth low-pass filter)

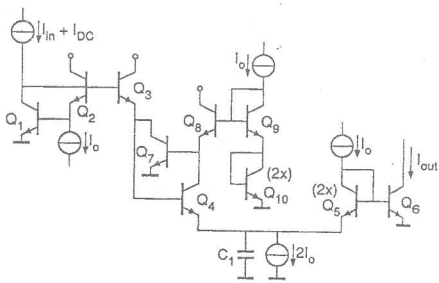
$I_{out}(2I_{C_1}I_{C_2} + 2I_{C_2}I_o + I_o^2) = I_{in}I_o^2$ (polynomial)

$$\begin{cases} 2I_{out}(I_{C_1} + I_o)P = I_{in}I_o^2 \\ 2(P - I_{C_2})(I_{C_1} + I_o) = I_o^2 \end{cases}$$ (TL-loop equations)

P = intermediate current

Step 4: Composition circuit

(Just one heuristically found solution)



Loops
- Q_1 through Q_6
- Q_7 through Q_{10}

Step 5: Replace ideal bias sources by realistic ones

Fig. 7, Illustration of the synthesis procedure for dynamic TL circuits

VIII TL oscillator

An example of a current-controlled oscillator, built up from two identical TL integrators is discussed below.

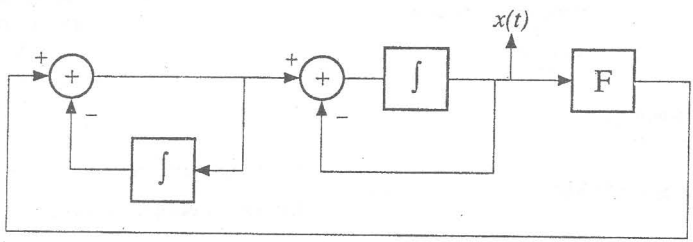


Fig. 8-1, Generic block diagram of a two integrator oscillator.

Fig. 8-1 depicts the block diagram, consisting of two integrators with unity feedback and some amplitude stabilizing function $F(x)$. Its output signal is $x(t)$. The circuit implements the second-order DE

$$\ddot{x}(t) + 2\omega\dot{x}(t) + \omega^2 x(t) = \dot{F}(x(t)) \tag{8-1}$$

A suitable form for F(x) is

$$F(x) = \frac{2Gx}{x^2+1} \text{ with } G > 1 \tag{8-2}$$

Substitution of (7-2) into (7-1) yields

$$\ddot{x}(t) + \omega\left(2 - 2G\frac{1-x^2(t)}{(1+x^2(t))^2}\right)\dot{x}(t) + \omega^2 x(t) = 0 \tag{8-3}$$

where the dot represents differentiation to time. In the stable oscillation mode the term between the large brackets in (8-1) vanishes and the DE reduces to its original form

$$\ddot{x}(t) + \omega^2 x(t) = 0 \tag{8-4}$$

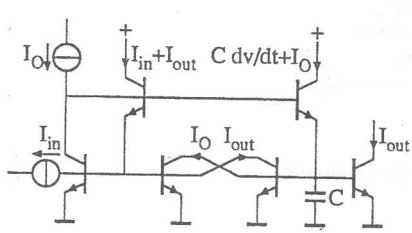


Fig 8-2 Seevinck's TL integrator.

The basic circuit of one of the TL integrators is shown in Fig. 8-2 and was first proposed by Seevinck [5]. The function $F(t)$ can easily be implemented by a *static* translinear circuit [2]. Finally, Fig. 8-3 depicts the complete circuit diagram (with ideal biasing sources).

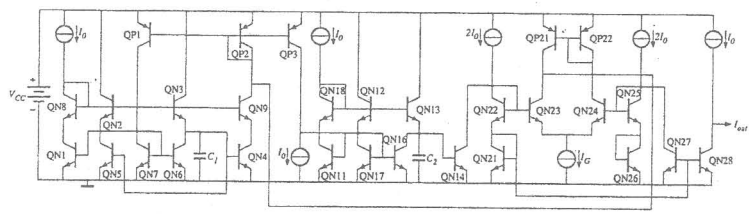


Fig. 8-3, Complete circuit diagram of the oscillator.

IX References

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