Piecewise-Linear GTO Thyristor Model

Lupco V. Karadzinov, M.Sc., Goce L. Arsov, Ph.D. and Lupco P. Panovski, Ph.D. Faculty of Electrical Engineering, St. Cyril and Methodius University, Karpos II b.b., P.O.Box 574, 91000 Skopje, Macedonia

ABSTRACT: In this paper we develop a simple piecewise-linear (PWL) gate-turn-off (GTO) thyristor model that correctly simulates internal physical processes and is suitable for obtaining analytical results for complex nonlinear phenomena in electronic circuits. The model is developed using two-transistor representation of the thyristor and PWL bipolar junction transistor (BJT) model for transient behaviour developed recently [1,2]. Unlike other models that simulate the transient response which are highly non-linear, our model is linear in all modes of operation and comprises of three resistances, six capacitances, three current dependent current sources, and three switches, one for each junction. The switches are 'on' when the corresponding junction is forward biased. The model GTO operation is demonstrated in thyristor phase-controlled rectifier. The main significance of the model is that its differential equations are linear in all regions of operation and can be represented in matrix form. This allows analytical results to be obtained for complicated nonlinear phenomena such as instabilities, subcharmonics, quasiperiodicity, intermitency and chaos [3].

I. INTRODUCTION

Gate turn-off thyristors (GTO) are efficient switching device that can handle high power like SCRs and can turn-off large currents with a gate signal. They are irreplaceable for high power industrial drives, like ac motor drives, induction heating, electric locomotives e.t.c. There are, reported in the literature, many thyrirstor models that have different advantages in allowing analysis or computer simulation of thyristor and circuits where it is implemented. The models are based on simulation of thyristor behaviour using controlled current and voltage sources[4,5,6], on its semiconductor physics [7,8,9]; or its two transistor representation [10,11,12]. The models of the first type are linear and easy to use in simulations and analysis, but they do not reflect the physical processes and are less accurate. The second two types give very good simulation results, but are strongly nonlinear having exponential nonlinearities and do not allow analytical results to be obtained for complicated nonlinear phenomena in power electronic circuits such as instabilities, subcharmonics, quasiperiodicity, intermitency and chaos [3].

In this paper we develop a piecewise-linear (PWL) gate turn-off thyristor model. It is based on the two transistor representation using recently developed PWL bipolar junction transistor (BJT) model for transient behaviour [1,2] suitable for obtaining analytical results for nonlinear phenomena. The BJT model has been developed from charge-control model which reflects the fact that instantaneous terminal currents are controlled by base-region minority carriers excess charge. Thus the thyristor model also represents physical processes, reproduces the transient behaviour accurately, it is PWL and can be represented in a matrix form to allow analytical results to be obtained.

With this paper we also show that it is possible to obtain simple GTO thyristor or any other bipolar semiconductor device PWL model for transient behaviour [1,2,13] using the charge control model and representing the stored excess minority carrier charge by a simple linear RC circuit for each junction.

II. GTO THYRISTOR MODEL DEVELOPMENT

Thyristor model developed here is based on the two-transistor representation of the thyristor shown in Fig.1a. For both BJTs (*pnp* and *npn*) we use the recently developed PWL BJT models for transient behaviour [1,2]. The *npn* BJT model with alpha parameters [1] is shown in Fig.1.b.

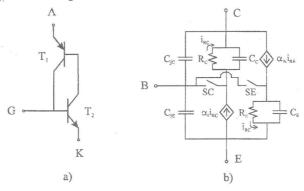


Fig.1. Basics for GTO thyrirstor model development: a) two transistor representation of the thyristor; b) PWL BJT transistor model for transient behaviour.

All BJT model elements are linear and two switches correspond to each junction. SE and SC are closed when corresponding junction voltages are directly biased, i.e. $u_{BE} > 0$ or $u_{BC} > 0$ respectively. The *pnp* BJT model can be obtained by the same scheme with operating the switches at opposite voltages, i.e. they are closed when $u_{EB} > 0$ or $u_{CB} > 0$. The new thyristor model is shown in Fig.2.

This thyristor model has four groups of switches, RC circuits and controlled current generators, which is more than the number of pn junctions. This is because the two collector junctions in the two transistor model represent the same junction (NsP) in the thyristor structure. To facilitate the reduction or merging of the duplicated elements we need to rearrange the switches' placement in the BJT model while still keeping its behaviour unchanged. This can be done by placing them between the RC circuits and the node that connects corresponding current generators and the rest of the model.

Now we have in parallel two RC-circuits (representing injected excess minority carriers charge from both sides of the NsP junction) which are connected to the rest of the circuit by switches closed simultaneously when the junction becomes forward biased ($u_{CBI} = u_{BC2} > 0$). Their resistance currents control two current sources (α_{II} and α_{IZ}). This part of the model is shown in Fig. 3.a.

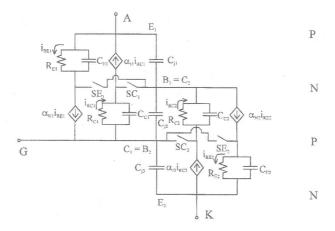


Fig.2. Thyristor PWL model for transient behaviour developed from PWL BJT model and two transistor analogy.

Two parallel RC circuits can be replaced by an equivalent one having resistance and capacitance values: $R_2 = \frac{R_{C1} \cdot R_{C2}}{R_{C1} + R_{C2}}$ and $C_2 = C_{C1} + C_{C2}$ as shown in Fig.3.b. To keep

the same behaviour of the model we must correct the transfer ratios of the current sources that depend on this RC circuits currents($\alpha_{\rm II}$ and $\alpha_{\rm I2}$). Since resistance R_2 now conducts both currents i_{RCI} and i_{RC2} , the new currents are given by following relations:

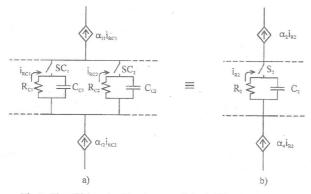


Fig.3. Simplifying the Thyristor model: a) The two parallel RC circuits of the NsP junction, b) Equivalent subcircuit and corrected transfer ratios.

$$\begin{split} \alpha_{I1} \cdot i_{RC1} &= \alpha_{I1} \cdot \frac{R_{C2}}{R_{C1} + R_{C2}} \cdot i_{R2} = \alpha_2 \cdot i_{R2} \\ \alpha_{I2} \cdot i_{RC2} &= \alpha_{I2} \cdot \frac{R_{C1}}{R_{C1} + R_{C2}} \cdot i_{R2} = \alpha_4 \cdot i_{R2} \end{split}$$

Other two current generators (α_{N1} and α_{N2}) can be substituted by only one that generates the same current α_{N1} i_{RE1} + α_{N2} i_{RE2}. Using this simplification we finally obtain the simple PWL GTO thyristor model shown in Fig. 4.

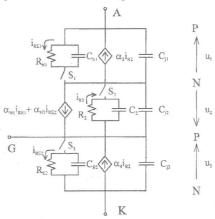


Fig.4. PWL GTO thyristor model with minimum elements.

III. SIMULATION RESULTS

The GTO operation of the model can be verified using any circuit simulation program because it comprises only linear circuit elements and switches. There is no need for a program that enables implementation of mathematical equations as is the case with other physical models. The circuit used is a simple half-wave phase-controlled rectifier shown in Fig. 5.

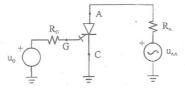


Fig. 5. Phase-controlled half-wave rectifier circuit.

Fig.6. shows simulation results when drive voltage u_{AA} is sine wave while the control signal at the gate terminal u_G is bipolar square pulse. The results verify that the model switches off when the gate voltage and current are negative. The reverse amplification ratio I_A/I_G is approximately 3.

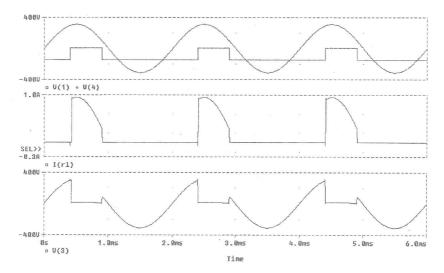


Fig. 6.: PSpice simulation of the circuit from Fig.5 with sine wave input voltage and bipolar gate pulses show gate-turn-off operation of the model.

IV. DISCUSSION

Thyristor model developed here is three dimensional circuit. It is linear in all modes of operation which allows its equations to be written in matrix form allowing further analysis and obtaining analytical results. The matrix form of the model differential equations reads:

$$\begin{bmatrix} \frac{du_1}{dt} \\ \frac{du_2}{dt_2} \\ \frac{dt}{dt} \\ \frac{du_3}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{S_1}{R_1(C_1S_1 + C_{J1})} & +\frac{\alpha_2S_2}{R_2(C_1S_1 + C_{J1})} & 0 \\ +\frac{\alpha_3S_2}{R_1(C_2S_2 + C_{J2})} & -\frac{S_2}{R_2(C_2S_2 + C_{J2})} & +\frac{\alpha_3S_2}{R_3(C_2S_2 + C_{J2})} \\ 0 & -\frac{\alpha_4S_2}{R_2(C_3S_3 + C_{J3})} & -\frac{S_3}{R_3(C_3S_3 + C_{J3})} \end{bmatrix} \cdot \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} + \begin{bmatrix} i_a \\ -i_a \\ i_a + i_g \end{bmatrix}$$

where $S_1=1$ when $u_1>0$; $S_2=1$ when $u_2>0$ and $S_3=1$ when $u_3>0$. This equation gives instantaneous junction voltages if anode and gate currents are known. All three voltages are needed only in tetrode thyristors, while in ordinary triode thyristors the terminal voltages will be: $u_G=u_1$ and $u_{AK}=u_1+u_2+u_3$. The same model developed here could have been obtained directly from the charge-control thyristor model. That would be much more complex procedure in comparison with the one presented here where we have used already existing PWL BJT charge-control model.

V. CONCLUSION

In this paper we have developed a simple PWL GTO thyristor model using charge-control PWL BJT model and two-transistor representation. The model has the simplicity of the behavioural models and has the accuracy of physical models since it also simulates internal physical processes. The model piece by piece linearity allows its matrix representation and thus allows further analytical results to be obtained.

An algorithm for parameter extraction from simple measurements or data sheet is still under development. The same procedure can be used to develop triac and other bipolar semiconductor devices.

References:

- [1] L.V. Karadzinov, G. L. Arsov, T.A. Dzekov and D.J.Jefferies. Charge-Control Piecewise-Linear Bipolar Junction Transistor Model: IEEE International Symposium on Industrial Electronics ISIE'96, 17-20 June 1996, Warsaw, Poland, pp. 561-566.
- [2] L.V. Karadzinov, G. L. Arsov, D.J. Jefferies and T.A. Dzekov. Beta-Parameters Charge-Control Piecewise-Linear Bipolar Junction Transistor Model. Proceedings of the 7th International Power Electronics and Motion Control Conference, Exhibition, Tutorials PEMC'96, 2-4 September 1996, Budapest, Hungary, Vol.1, pp. 161-165.
- [3] Y. Yasuda. Electronic chaos in silicon thyristors. Japan Journal of Applied Physics 1, 33(1B):594'598, Jan. 1994.
- [4] Da-Guang Ni, Gerard Rojat, Guy Clerc and Jean-Pierre Chante. Numerical Modelling of Gate Turn-off Thyristor Using SICOS. IEEE Transaction on Industrial Electronics, Vol. 40, No. 3, June 1993, pp. 326-332.
- [5] Y. C. Liang and V.J. Gosbell. Transient Model for Gate Turn-off Thyristor in Power Electronic Simulations. International Journal of Electronics, 1991, Vol. 70, No. 1, pp 85-89.
- [6] N. A. Losic. Modelling of Thyristor Circuit in Computer-Aided Analysis and Design. Third Annual IEEE Applied Power Electronics Conference and Exposition APEC'88, 1-5 Feb. 1988, New Orleans, Louisiana, USA, pp. 219-225.
- [7] Cliff L. Ma and P.O. Lauritzen. A Physics-Based GTO Model for Circuit Simulation. IEEE Power Electronics Specialists Conference - PESC'95, Atlanta, Georgia, USA, June 18-22, 1995, pp.872-878.
- [8] Ranadeep Dutta, Cheanlung Tsay, Allen Rothwarf and Robert Fishl. A Physical and Circuit Level Approach for Modelling Turn-Off Characteristics of GTO's. IEEE Transaction on Power Electronics, Vol. 9, No. 6, November 1994, pp. 560-566.
- [9] P. R. Palmer and K. J. Tseng. An Accurate GTO Model for Circuit Simulations. 5th European Conference on Power Electronics and Applications, Brighton, UK, September 1993, Vol. 2, pp 244-248.
- [10] M. Bayer, R.Kraus and K. Hoffmann. A New Analytical GTO-Model for Circuit Applications. IEEE Power Electronics Specialists Conference - PESC'95, Atlanta, Georgia, USA, June 18-22, 1995, pp.879-885.
- [11] R. L. Avant and F. C.Y. Lee. A Unified SCR Model for Continuous Topology CADA. IEEE Tran. on Industrial Electronics, Vol. 31, No.4, Nov. 1984, pp. 352-361.
- [12] B. W. Williams. State-Space Thyristor computer model. Proceedings of IEE, Vol. 124, No. 9, Sep. 1977, pp.743-746.
- [13] L.V. Karadzinov, D.J. Jefferies, G.L. Arsov and J.H.B. Deane. Simple Piecewise-Linear Diode Model For Transient behaviour. International Journal of Electronics, 1995, Vol.78, No. 1, 143-160.