# A smart thermocouple interface and voltage processor

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**Abstract:** This paper presents a novel interface for voltage-generating sensors, such as thermopiles and thermocouples. The processor converts sequentially a DC input voltage and three internally generated voltages into a period-modulated square-wave output signal. The internal signals are required to provide auto-calibration for offset and gain and to measure the interface internal temperature. Dynamic Element Matching is applied to generate an accurate and reliable PTAT voltage. The applied modulator used in the circuit has a 2nd-order filtering which suppresses low-frequency (1/f) noise. This filtering property enables the use of a low-cost CMOS process for the implementation of the circuit. The interface is able to measure a voltage ($V_x$) in the range of -27 mV to 100 mV, the measured accuracy of the system over a temperature range of -25°C to 75°C is 550 ppm of $V_x$. The inaccuracy in determining the reference-junction temperature is 0.6 K. The measuring time is ≤ 50 ms.

## 1. Introduction

This paper presents a novel design and implementation of an interface for DC voltage sources. The interface is capable to condition the signals of thermocouples and of a built-in temperature sensor. The output signal is readable by a micro-controller. To insure the accuracy and reliability of the circuit, auto calibration for offset and gain, is applied. The interface acts as an asynchronous converter for DC voltages employing a relaxation oscillator whose output is a period-modulated signal. Only one wire is needed between the micro-controller and the interface. The micro-controller converts the period-modulated signal into a digital number by simply counting the number of pulses within each period. Finally, from the obtained data, the micro-controller calculates the measuring-junction temperature of the thermocouple.

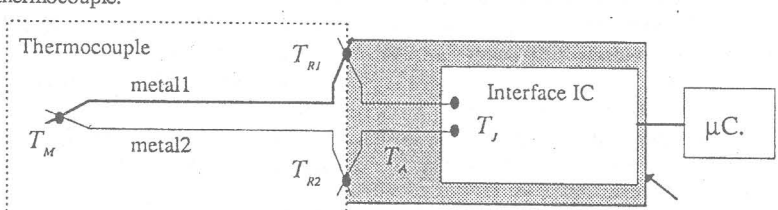


**Fig. 1 The system set-up**

The system set-up is shown in Fig. 1. The interface measures the thermocouple signal ($V_x$) which is directly related to the difference between the measuring-junction

temperature ($T_M$) and the reference-junction temperature ($T_{R1}=T_{R2}=T_R$) of the thermocouple. The interface also measures its own temperature $T_j$ to compensate for the reference temperature of the thermocouple. Due to the self heating, the internal temperature of the interface is higher than the ambient temperature $T_A$. This limits the maximum allowable power dissipation. The reference temperature of the thermocouple is kept equal to the ambient temperature, by fixing the reference-junction and the interface with a low mutual thermal resistance at a high-thermal-capacity object, as indicated in Fig. 1, so that $T_R \approx T_A \approx T_j$. The thermocouples themselves are absolutely offset-free. Therefore any additive error degrades the performance. This is especially important for small measurement ranges of ($T_M$-$T_R$). For the larger ranges it is desirable that the maximum error of the interface is less than that of the thermocouple itself. The relative accuracy for different types of thermocouples is in the range of ±2500 ppm to ±7500 ppm [1].

## 2. Measuring approach

In addition to the thermocouple voltage, the interface generates two other voltages internally. One is a base-emitter voltage ($V_{BE}$) and the other is a PTAT voltage ($V_{PTAT}$). Both $V_{BE}$ and $V_{PTAT}$ are temperature dependent. Linear combinations of these two voltages are used to obtain a reference signal ($V_{ref}$) and a temperature-dependent signal ($V_T$), as follow [2] :

$$V_{ref} = V_{BE} + c_1(V_{BE2} - V_{BE1}) = V_{BE} + c_1 V_{PTAT} = V_{BE0} \qquad (1)$$

$$V_T = V_{BE} - c_2 V_{PTAT} = \frac{V_{BE0}}{T_r}(T - T_r) \qquad (2)$$

where $T_r$ is the temperature at which $V_T$=0, and $V_{BE0}$ is the extrapolated value of the linear approximation of $V_{BE}$ at 0 K, as indicated in Fig. 2.

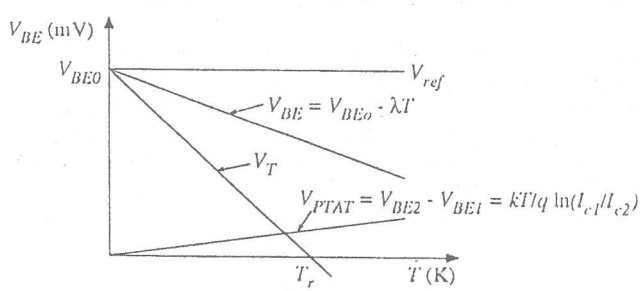


**Fig. 2 A linear approximation of $V_{BE}$ versus $T$ for three transistors operating at different collector-current densities.**

In Fig 3(a) the measurement set-up is shown. A divider is used to divide $V_{BE}$ by a constant division factor ($\alpha_d$ ) to make the voltage ($V_{BE}/\alpha_d$ ) fitting within the range of ($V_{PTAT}$ and $V_x$). The interface converts the four basic voltages $V_{ex}$, $V_{PTAT}$, $V_{BE}/\alpha_d$ and $O_{ff}$ to the time domain using a linear voltage ($V$) to period ($t$) converter. The output voltage of this converter (Fig. 3(b)) is period modulated in such a way that $t_{ap} = a(O_{ff} + V_{pi})$, where $O_{ff}$ and $a$ are the equivalent offset and the conversion factor of the system, and $V_{pi}$ (i = 1,...4) represents the four basic voltages to be converted.

Since the basic voltages are converted in an identical way to time intervals, it becomes possible to implement the algorithms (1) and (2) by the μC in the time domain. Moreover, the three-signal technique [2] can be applied to find the following dimensionless ratios:

$$M_1 = \frac{\left(t_x - t_{off}\right)}{\left(\alpha_d t_{BE} + c_1 t_{PTAT}\right) - \left(\alpha_d + c_1\right) t_{off}} = \frac{V_x}{V_{ref}}, \tag{3}$$

$$M_2 = \frac{\left(\alpha_d t_{BE} - c_2 t_{PTAT}\right) - \left(\alpha_d - c_2\right) t_{off}}{\left(\alpha_d t_{BE} + c_1 t_{PTAT}\right) - \left(\alpha_d + c_1\right) t_{off}} = \frac{V_T}{V_{ref}}. \tag{4}$$

In these ratios the influence of the additive and the multiplicative parameters ($a$ and $V_{off}$) are eliminated, and the only requirement for the converter is that of linearity.

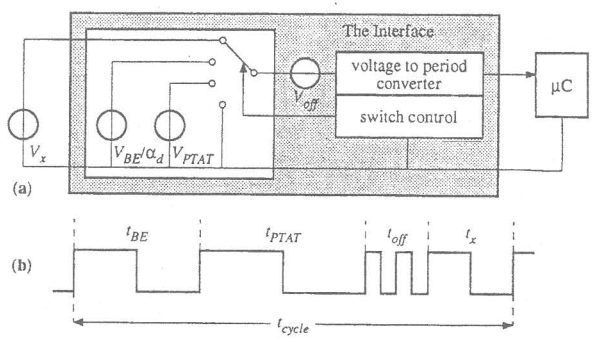


**Fig. 3(a) Measuring approach of the interface, (b) the period-modulated output signal.**

Once the ratios $M_1$ and $M_2$ are found. the μC calculates the measured thermocouple signal ($V_x$) by multiplying $M_1$ by $V_{ref}$, from which the temperature difference ($T_M$-$T_R$) of the thermocouple is found using a look-up table for the values of the thermocouple voltages and the corresponding temperature differences. Similarly, $V_T$ is found by multiplying $M_2$ by $V_{ref}$, from which the interface temperature ($T_J$) is calculated using (2). Since the reference-junction temperature of the thermocouple ($T_R$) is approximately equal to the internal temperature of the interface ($T_J$), the measuring-junction temperature can simply be found using: $T_M \approx T_J + (T_M - T_R)$.

# 3. Generation of $V_{PTAT}$ and $V_{BE}$ using DEM

An accurate PTAT voltage is generated by a novel application of Dynamic Element Matching (DEM) [3]. The principle of this method is shown in Fig. 4. The transistors $M_1$ - $M_4$ represent four current mirrors. One of these transistors supplies current to the bipolar transistor $Q_1$ while the other three supply current to $Q_2$, so that the current ($I_{c2}$) passing through $Q_2$ is three times the current ($I_{c1}$) passing through $Q_1$. The difference between the base-emitter voltages $V_{BE2}$ and $V_{BE1}$ represent the PTAT voltage.

$$V_{PTAT} = V_{BE2} - V_{BE1} = \frac{kT}{mq} \ln \frac{I_{c2} I_{s1}}{I_{c1} I_{s2}} \tag{4}$$

where $I_{s1}$ and $I_{s2}$ are the saturation currents of $Q_1$ and $Q_2$ respectively and m is the emission coefficient whose value is slightly less than one [4]. In our CMOS interface for the vertical PNP substrate transistors we experimentally found that m≈0.992.

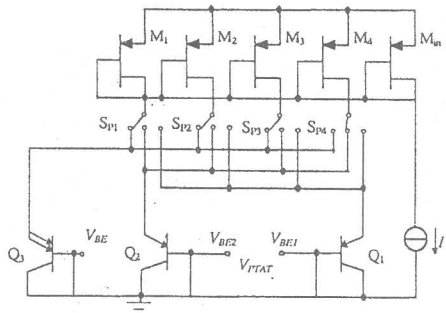


**Fig. 4 Generation of $V_{PTAT}$ using DEM, according to [3].**

The effect of any mismatch in the characteristic of the transistors $M_1$-$M_4$, which would cause a deviation in the value of $V_{PTAT}$, is strongly reduced by interchanging the positions of $M_1$-$M_4$. Furthermore, in order to eliminate the mismatch in the transistors $Q_1$ and $Q_2$ , their position are interchanged as well. There are eight switching possibilities. The average value of $V_{PTAT}$ over these eight switching phases is almost equal to $(kT/mq)\ln 3$, even when there is some mismatching between the transistors.

**Example:** For $\Delta I_s/I_{s2}=\pm 0.01$, the relative inaccuracy $\Delta V_{PTAT}/V_{PTAT}$ is zero whereas, without applying DEM, the error amounts to 0.9%.

An additional advantage of using the DEM technique to generate $V_{PTAT}$ is that the low-frequency noise of the current mirrors is reduced as well. This is an important contribution towards filtering out the flicker noise of the CMOS transistors. To take full advantage of this filtering it is required that the corner frequency is less than the cycling frequency of the generated $V_{PTAT}$ voltage. This can be achieved by choosing the appropriate dimensions for the CMOS transistors.

In the circuit shown in Fig. 4, a multi-emitter transistor ($Q_3$) is used to get a base-emitter voltage ($V_{BE}$) which can be calibrated by trimming its emitter area. The switching positions are controlled in such a way that, during the measuring phase of $V_{BE}$, the current flowing in $Q_3$ is constant and equal to $2I$. The base-emitter voltage versus temperature ($V_{BE}(T)$) can be approximated by:

$$V_{BE} = V_{BE0} - \lambda T - \frac{1}{2}(\eta - x)\frac{kT_r}{q}\left(\frac{T-T_r}{T_r}\right)^2 \qquad (6)$$

where $\lambda$ represents the slope of the tangent of the curve at the point $V_{BE}(T_r)$ and $x$ is an exponent describing the temperature dependence of the collector current $I_c$ according to $I_c=cT^x$. In [5] for the parameters $V_{BE0}$ and $\eta$ of NPN transistors the empirical values of respectively 1262.6 mV and 3.54 are found. To our experience the values for CMOS substrate transistors are close to those of the NPN transistors.

Some spreading in the value of in the $V_{BE}$ voltage will occur, due to the process tolerance and the inaccuracy of the bias current ($I_c$=2I) This spreading can be compensated for by adjusting the emitter area for the desired value of $\lambda$. Some compensation of the non-

linearity of $V_{BE}$ is performed in software by the micro-controller: In the compensation algorithm the non-linear behaviour of $V_{BE}(T)$ is approximated with the piece-wise linear characteristics shown in Fig. 5(a), which results in the reduced nonlinearity depicted in Fig.5(b).

For good A/D resolution, the signals to be converted have to be in the same range. In other words, the low level signals ($V_{PTAT}$ and $V_x$) have to be amplified and/or the relatively large signal ($V_{BE}$), which is 20 times greater, has to be attenuated. Because of its simplicity the attenuation method is preferred.. It can be shown that this attenuation hardly effect the system signal-to-noise ratio. The absolute accuracy of a passive voltage divider depends on components matching. Even when laser trimming techniques are used to achieve the required accuracy, long-term stability is not guaranteed, because of ageing effects. Therefore, DEM technique for voltage division is applied, using a novel voltage divider, proposed in [7].

## 4. Realization

The schematic diagram of the interface circuit, shown in Fig. 6(a), contains the following main parts:

- A first-order oscillator to convert the analogue signals to be measured into a period-modulated signal.
- A circuit to generate the two voltages ($V_{PTAT}$ and $V_{BE}/\alpha_d$) required to obtain the reference and the temperature-dependent signals.
- A logic circuit to control the phase selection and the switching operations of the interface and to start up oscillation.
- A circuit to generate the alternating integration current.

Dynamic element matching is applied to obtain a high accuracy for the attenuation factor $\alpha_d$ and of the generated PTAT voltage $V_{PTAT}$ [3] - [5]. The micro-controller measures the duration of each phase and calculates the ratios $M_1$ and $M_2$ using Equations (3) and (4). To enable the micro-controller to identify the different phases of the output signal, it is necessary to synchronise the interface and the micro-controller. One method to do this is to enable the micro-controller to identify the offset phase, by making the interval of the offset pulse shorter

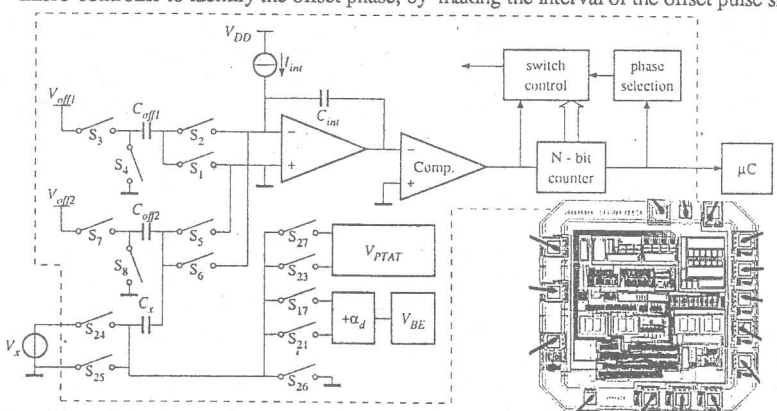


**Fig. 5(a) Schematic diagram of the interface, (b) a photomicrograph of the chip.**

than the intervals of the others, The offset pulses is doubled to achieve that $t_{off}$ is not beyond the range of the other intervals. A logic circuit is required to control the phase selection and the switching operations of the circuit.

## 5. Measurements and results

The complete circuit is realised on a single chip in a 0.7 µm CMOS process. The chip area, for the total IC including its bond pads, is 3.2 mm$^2$. A photomicrograph of the chip is shown in Fig. 4(b). The applied µC is of the type D87C51F8 with internal 8 Kbytes EPROM and 256 bytes RAM, the clock frequency is 12 MHz and the sampling frequency of the µC is 3 MHz. The digital output signal of the interface is applied as input to the µC. The data available from the µC are applied to the computer, by which the calculations of the ratios $M_1$ and $M_2$ according to (3) and (4) and the calculations of the input signal and the reference junction temperature are performed. Before making the measurement test for the interface, the base-emitter voltage is calibrated by using an accurate test voltage as an input signal. The value of this voltage is calculated using the data provided by the µC which correspond to the output signal of the interface. The emitter area is adjusted such that the calculated voltage is as close as possible to the applied test voltage. After the calibration of the base-emitter voltage, voltage and temperature measurements have been performed to check the accuracy of the circuit in measuring the thermocouple signal and its own temperature. To test the interface an accurate test voltage ($V_x$) is applied to the input of the chip. The measured scaled error is found to be -550 ppm of $V_x$. This error is due to the inaccuracy of the internal bandgap reference. Although the interface has been designed for the voltage range of (-27 mV to 100 mV), large positive values of $V_x$ up to +500 mV can be applied as well without a

*Table 1 The main measurement results*

| parameters | value | | |
|---|---|---|---|
| Supply voltage | 3.5- 6 V | | |
| Input voltage range | -27 + 500 mV | | |
| Measurement time | 50 ms | | |
| Power dissipation | 4 mW at 5 V | | |
| | 250 K | 300 K | 350 K |
| inaccuracy in $V_x$ | 550 ppm | | |
| $\sigma_{Vex}$, due to noise | 0.013 mV | 0.014 mV | 0.013 mV |
| inaccuracy in $T_R$ | 0.6 K | | |
| $\sigma_{TR}$, due to noise | 0.06 K | 0.05 K | 0.05K |

decrease of the relative accuracy. Also the accuracy of the internal temperature sensor has been tested. The inaccuracy of this sensor was found to be 0.6 K over the temperature range of -25°C to + 75°C. Table 1 list the main measurement results at room temperature and at the temperature extremes (250 K and 350 K) of the chip.

## 6. Conclusion

A low-cost interface for a thermocouple has been designed and realised using a CMOS process. The main properties of this interface are its ability to measure small input

voltages together with its own temperature. Moreover, the application of the three-signal technique in the measuring approach has guaranteed the accuracy and long-term stability against the deviation in the offset and gain. Also the application of a special DEM has enabled the generation of an accurate and reliable $V_{PTAT}$.

The main causes for the limited accuracy in the measured results are the inaccuracy of the generated base-emitter voltage and the deviation of the reference junction temperature of the thermocouple from that of the interface itself due to self heating. The change in $V_{BE}$ due to the inaccuracy in the reference current and the process parameters is reduced by calibrating a transistor with multi-emitter area, while the inaccuracy due to the non-linearity is limited by applying a specific method in processing the signal by the micro-controller. The error of the internal temperature sensor amounts to 0.6 K for a power dissipation of about 4 mW.

The application of an oscillator with $2^{nd}$-order filtering to suppress the low-frequency (1/f) noise has enabled the use of low-cost CMOS process for the implementation of the circuit.

## REFERENCES


[1] "Manual on the use of thermocouple in temperature measurement," American Society for testing and materials, Fourth printing, April 1987.

[2] G.C.M. Meijer, J. van Drecht, P.C. de Jong and H. Neuteboom. " New concepts for smart signal processors and their application to PSD displacement transducers," Sensors and Actuators, no. 35, pp. 23-30, 1992.

[3] G.C.M. Meijer, Patent appl. 1000222, April 1995.

[4] F.M.L. van der Goes, G.C.M. Meijer "A simple and accurate dynamic voltage divider for resistive bridge transducer interfaces," in Proc. of IMTC., Hamamatsu, Japan, May 1994, pp. 784-787.

[5] F.M.L. van der Goes, "Low-cost sensor interfacing," Ph.D. thesis, Delft University of Technology, Electronics Research Laboratory, April 1996.